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Chapter 6

Electronics, data acquisition and database

6.1 Overview

This Chapter describes the systems which digitize the electrical signals from the photodetectors and select events of interest for mass storage and physics analysis. The database is also described in this chapter. It maintains permanent records of the construction, installation and history of the experiment. It is used by all other subsystems and is essential to the offline data analysis.

In addition to digitizing the signals from the photodetectors, the electronics systems supply the high voltages to the photodetectors and provide monitor and control functions. Information from the monitoring systems is regularly recorded in the database to provide a history of the experiment; faults and errors detected by the monitoring systems are logged to the database as and when they occur. The configuration of the database and the types of information recorded are discussed further in Section 6.7. Many of the monitoring functions are provided by processors embedded in the main electronics systems and are described with those systems.

The principal function of the electronics and DAQ system is to digitize and record the signals from the photodetectors; the following steps are involved:

- The time and the charge of each pulse from the photodetectors exceeding a (programmable) threshold of 0.3 photoelectrons is measured and digitized as a hit by the front end units. The hit information is time-ordered and passed from the front end units over a network to the central system and trigger farm. The central system and the trigger farm together time-order the entire data stream and divide it into partially overlapping time blocks. The processors in the trigger farm examine the data in units of single time blocks and apply a software trigger algorithm to separate the interesting events from noise.
- Finally hits from real events are passed to the data acquisition system which provides data storage, run control and user interfaces.

The functions of the other system, which aren't in the direct readout chain are the:

- Supply clean, programmable high voltage to the photomultiplier tubes. Provide a stable clock signal to the front-end boards which is synchronized with GPS. Have the parameters of the construction and operation of detector readily available for the analysis programs in a database. A detector monitoring and control system to monitor the condition of the detector and its environment, record these values and notify the operator in case of a problem.

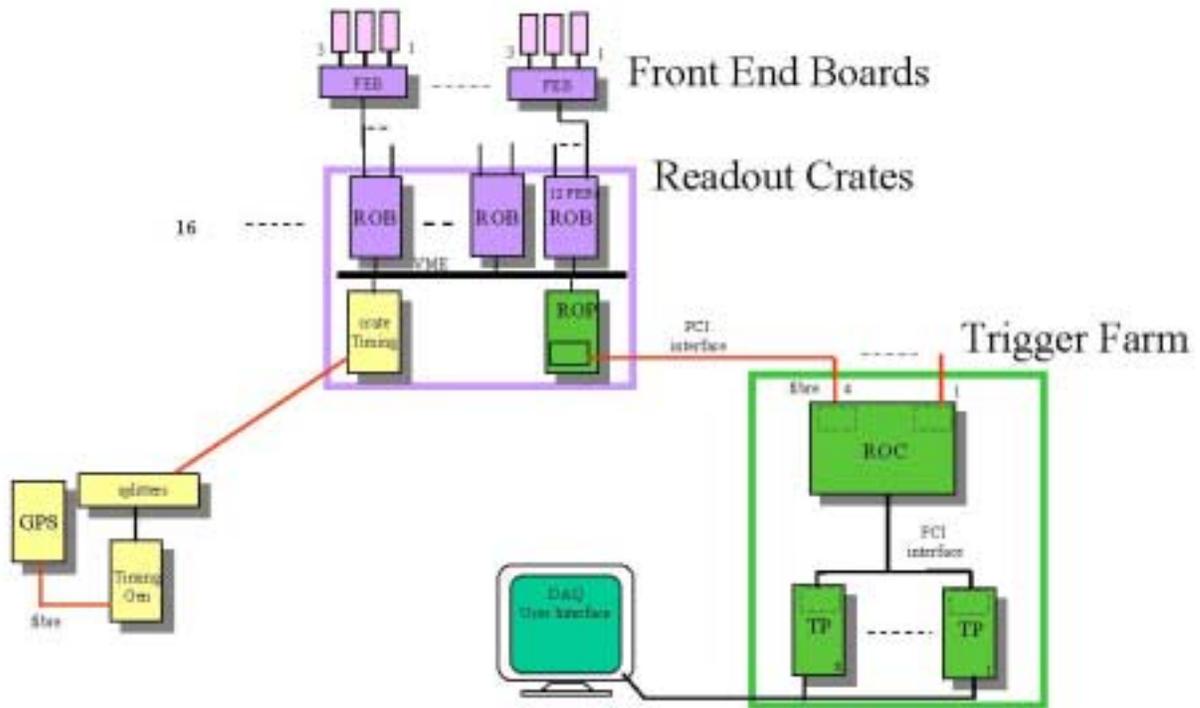


Figure 6.1 Schematic diagram of the principal components and organization of the electronics system.

Figure 6.1 shows the principal components of the electronics system. The overall architecture for the near and far detectors is very similar although they differ in the details of the front-end board and its readout board. These are described in detail in sections 6.3 and 6.4

6.1.1 Physics Requirements

The primary physics measurements in the MINOS experiment rely upon the:

1. measurement of the length of events to differentiate between NC and CC neutrino interactions;
2. reconstruction of long muon tracks for momentum measurement by range or magnetic deflection;
3. differentiation between electromagnetic and hadronic showers by their characteristic longitudinal and transverse energy deposition profiles;

4. calorimetric measurement of hadronic and electromagnetic energy; and
5. recognition of certain simple event topologies characteristic of τ decays.

The provision of timing measurements with sufficient accuracy to determine the direction of a track will allow an extension of the physics capabilities of the far detector to studies of upward-going muons from neutrino interactions in the surrounding rock and atmospheric neutrino interactions in the detector.

The calorimetric energy measurements and the separation of hadronic and electromagnetic showers rely upon the proportionality of light-yield to deposited energy. Figure 6.2 shows distributions of the maximum pulse heights, in terms of photoelectrons, that would be recorded for electron neutrinos with the same energy spectrum as the muon neutrinos in the highest energy neutrino beam. The maximum signal to be recorded to achieve electromagnetic calorimetry over the entire energy range is equivalent to a 200-250 photoelectron signal from the photodetectors. The maximum signal to be recorded by the electronics has been set at the equivalent of 150 photoelectrons for a photodetector channel with normal gain. Monte Carlo studies have shown that this is sufficient to get an unsaturated measurement from at least one of the side of the fiber readout.

Because it is important to maintain high efficiency, the effective thresholds must be set at the equivalent of 0.3 photoelectrons (pe) or less for all channels. The front-end noise must therefore be kept to a small fraction of the single photoelectron signal for a low gain channel. The electronics must have sufficient dynamic range and low noise to handle the maximum signals on normal channels and to resolve the smallest signals of interest from low gain photodetector elements [1].

The event rate of ~ 200 interactions per $10 \mu\text{s}$ spill in the entire near detector is relatively high although the interactions are distributed uniformly along the detector. The single channel will see 1-2 hits during this spill and shaping and dead times must therefore be sufficiently short that the pileup of hits and deadtime losses on a single channel are negligible.

The times of hits must be recorded with sufficient accuracy (19 ns, the Main Injector RF frequency) to enable events which overlap in one or both views to be resolved using timing 6-4 information. The ability to flag hits potentially corrupted by pileup from a previous hit on the same channel is desirable, as is the ability to examine the history of the detector for a few microseconds before the time of an event.

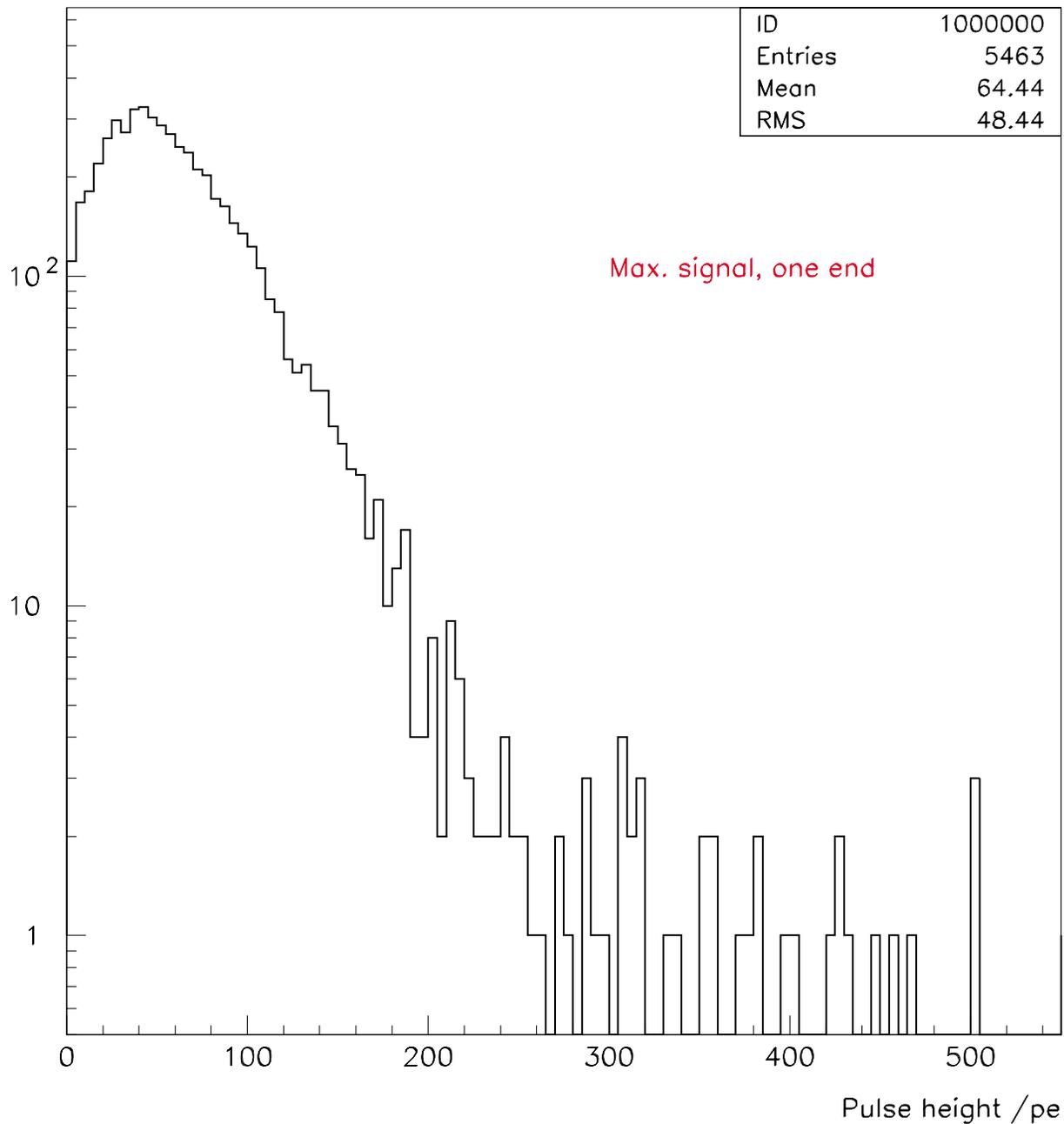


Figure 6.2 Distributions of the maximum pulse heights (in terms of photoelectrons) for interactions of electron neutrinos with the energy spectrum of the highest energy NuMI beam.

Cosmic ray muons will be the main method of cross-calibrating the energy scales of the near and far detectors. It is therefore important that both detectors are able to record cosmic ray muon tracks. The flux of cosmic ray muons at the near detector (~ 300 Hz)[2] is expected to be ample for this purpose; the relatively low muon flux at the far detector (~ 1 Hz) means that the detector must be sensitive for a high fraction of real time.

The systematic differences between the two detectors must be understood, and having different front end electronics in the near and far detectors is a concern, but previous experience with upgrading the CDF detector electronics without changing the detector itself has shown that systematics associated with different electronics can be understood to the 1% level with careful calibration and study. This should be adequate for the MINOS experiment. Both systems will have internal calibration systems and the light flasher will also be used.

Dark count rate per mm ² of photocathode	3 Hz
Far detector maximum rate/channel	122 Hz
Far detector typical rate/channel	62 Hz
Far detector total rate	1.4 MHz
Near detector maximum rate/channel	136Hz
Near detector typical rate/channel	28 Hz
Near detector total rate	0.3 MHz

Table 6.1 Expected singles rates in the MINOS detectors due to radioactivity and photocathode dark counts for a threshold that detects 1 photoelectron. 8-fold optical summing is assumed for the far per-channel rates.

The absolute rate of beam neutrino interactions at the far detector is extremely low (about 1 mHz) and to control possible backgrounds from cosmic ray interactions it is important to associate an event with the 10 μ s spill of the Main Injector. This can be achieved by recording the absolute times of events to $\ll 1$ ms and correlating the event time with the times of machine spills recorded at Fermilab.

Since the thresholds must be low to ensure high efficiency, the singles rates in the two detectors will be determined by radioactivity in the cavern rock and in the detector steel, and the dark-counts from the photodetectors, which are predominantly at the level of a single photoelectron. The total counting rate above a threshold of 0.3 photoelectrons due to radioactivity is estimated to be 510 kHz for the far detector and 145 kHz for the near detector [3, 4, 5]. The photodetector dark-count rate has been measured to be ~ 3 Hz per mm² of photocathode although it is rather sensitive to temperature. Singles rates are shown in Table 6.1, for the nominal dark-count rate. All the single-channel rates are very low; the higher rates are associated with channels connected to strips at the outside of the detector. Because of the large number of channels the overall total rates are high. Since

there is still some uncertainty about the dark-count rates, the electronics has been designed to handle a maximum rate of 5 Mhit/s for the far detector and 2.5 Mhit/s for the near detector, a safety factor of 3 over the worst-case rates. The design of the back-end of the system can easily be scaled down, with a consequent saving in cost if the rates prove to be less.

Because the experiment will rely upon a detailed comparison of the characteristics of events recorded in the near and far detectors, it is important that the electronics be accurately calibratable.

6.1.2 Minimizing potential noise sources

The front-end electronics must digitize low-level signals. There are a number of potential electrical noise sources at both detector sites the magnet coils, the lights and high-current electrical apparatus such as pumps, the cranes and ventilation fans, all of which could introduce noise into the front-end of the system, either by radiation, induction or currents flowing in 'ground loops'. Care must be taken both in the design and the installation of the electronics and other detector components to ensure that the effects of these sources of noise are minimized.

The power distribution systems in the Soudan cavern and near detector hall are described elsewhere [6, 13]. The power for the ventilation system, the magnet coils, general use (e.g., welding) will be isolated from the power for the electronics by means of separate transformers. 'Quiet' AC power for the electronics will be supplied from shielded transformers. The power and ground lines from these transformers will run in separate conduits to circuit breakers and thence to receptacles mounted close to the electronics racks. The ground lines for this power will be isolated and run back to a common grounding point at the transformers. This 'quiet power' will be used only for electronics, computers and some test equipment, but not for high power devices such as pumps, large fans or welding apparatus.

Separate power distribution and grounding systems will be provided for the high current electrical apparatus. The latter will consist of loop of thick copper wire embedded in the concrete floor slabs. Attachment points to the grid will be provided so that short connections can be made between the apparatus and a low impedance path to the main power ground. The fluorescent lights will have electronic ballasts and filtering to minimize radiated noise, which is especially important as they start to reach the end of their lifetime.

The power supplies for the magnet coils are another potential source of noise. Power for the coils will be supplied from transformers used only for this purpose. Whilst it would be desirable to use linear power supplies for the magnets, the high current (40 kA) for the near detector coil, and efficiency and heat load considerations at the Soudan site, force the use of SCR controlled supplies at both locations. Sufficient filtering of the magnet supplies will be provided to eliminate the high frequency spikes from the SCRs, which are the main concern.

The small size of the photodetectors and sensitive portion of the electronics makes them inefficient antennae at the frequencies of the noise radiated by electric motors and welders.

During the installation and operation phases care will be taken to ensure that the quiet power grounds are not inadvertently connected to grounds used by other pieces of apparatus or to the detector steel plates and support structures. Tests of this isolation will be part of the installation procedure.

With proper attention paid to the control of the grounding, noise is not anticipated to be a problem.

6.2 Requirements and performance criteria

The electronics and data acquisition systems for the MINOS detector will operate in a continuously-sensitive ‘triggerless’ mode. The selection of events for physics analysis and calibration will be performed by software in one or more processors. The primary functions of the system are:

1. To record:
 - a. neutrino events during the Main Injector spill and
 - b. cosmic ray events in the time between Main Injector spills.

The recorded data consist of the amplitudes and absolute times (derived from a clock synchronized to the GPS system) of all pulses from the photodetectors above a programmable threshold.

2. To record calibration pulses from:
 - a. the charge-injection system for calibration of the electronics system, and
 - b. the laser light calibration system for calibration of the photodetection system.
3. To record, or automatically subtract, ADC pedestal values.
4. To monitor components of the readout and other systems and log fault conditions.
5. To log environmental conditions.

The performance requirements for the electronics systems are shown in Table 6.2.

6.2.1 Architecture

The electronics uses a simple continuously-sensitive readout architecture. The times and amplitudes of all signals from the photodetectors above a pre-set threshold are digitized, ‘stamped’ with real-time and sent to processors in a ‘trigger farm’ where a software trigger is implemented. The trigger algorithms that have been studied select events by correlating hits first in time and then space. The use of processors, rather than a hardware trigger, allows great flexibility and event selections could, for example, be made based on the pulse height of hits. The events selected by the processors are then passed on to the data acquisition system for any further analysis or selection and subsequent mass storage.

Such a triggerless readout scheme has the advantage that a large degree of flexibility is retained for the eventual event selection algorithm and does not require the

complexities of programmable trigger logic or the distribution of fast trigger signals over a physically large distance. Data links with the necessary bandwidth and the processors necessary to implement such a triggerless system are currently available commercially. They are relatively inexpensive and since this is a rapidly developing area of technology it is likely that future commercial developments will reduce costs in the next few years.

The principal components of the electronics system are shown in Figure 6.1. They are:

1. front end units;
2. front end readout crate;
3. trigger farm hardware;
4. trigger farm and event selection software, and
5. GPS timing system.

Parameter	Near Detector	Far Detector	Comments
Spill length	8 μ s	8 μ s	Neutrino spill The far detector must have >80% duty cycle for cosmic ray muons out of spill for calibration.
Repetition time	≥ 1.9 s	≥ 1.9 s	Essential for calibration.
Cosmic muon rate	~ 300 Hz	~ 1 Hz	
Number of channels	9,408	23,232	Assumes PMT gain of 10^6
Threshold	≤ 0.3 pe	≤ 0.3 pe	
Front-end rms noise	≤ 0.05 pe	≤ 0.05 pe	
Charge measurement range	0.005 - 24 pC	0.005 - 24 pC	
Digitization accuracy	5%	5%	Resolve overlaps in near detector; not critical for far detector.
Time resolution (1)	19 ns	--	
Time resolution (2)	--	1.5 ns	For atmospheric ν and upward/downward muon separation in far detector.
Single channel deadtime	0 during spill	<10 μ s	Pileup and losses in near detector; not critical for far detector.
Preamp charge injection Single-channel disable	0.005 - 25 pC	0.005 - 24 pC	Remove bad channels from readout.
GPS-based clock	<1 μ s	<1 μ s	Associate events with real time of MI spill.

Table 6.2 Parameters for the MINOS electronics system.

The numbers of each component are given in Table 6.3; their functions are now described in detail.

Component	Near Detector	Far Detector	Comments
PMTs	147	1472	16 Channel PMTs – Far 64 channel - Near
Front-end Boards	588	491	16 chs N.D. 36 chs F.D.
Readout Crates	16	16	
Readout Boards	74	41	128 chs N.D., 432 chs F.D.
Front-end Processors	16	16	VME Single Board Comp.
FE Timing Card	16	16	
Trigger Farm Crate	1	1	
Input Processor	1	1	
Farm Processor	<5	<5	
Output Processor	1	1	
Timing System			
GPS	2	1	
Passive Clock Fanout	2	2	

Table 6.3 Lists the numbers of each component in the readout system.

5.3 Near Front Ends (WBS 2.3.1)

5.3.1 Introduction

The Main Injector is being designed for high beam intensities which can produce one or more event in the Near Detector in each RF bucket during the spill. In order to reconstruct each event accurately, it is necessary to be able to associate every event with a particular RF bucket. This requires very fast electronics, capable of digitizing at the 53 MHz RF frequency. Furthermore, since the spill may last for $\sim 10 \mu\text{s}$, it is desirable that there be no deadtime during the spill, so that every event that occurs during the spill is measured and recorded. The electronics for the Far Detector does not need to operate at this high rate, and it would be overkill to put fast electronics in the Far Detector. For a given dynamic range and accuracy, fast electronics with low deadtime is generally more expensive than slow electronics. Since there are twice as many channels in the Far Detector as in the Near Detector, there is a significant cost advantage in having fast electronics only in the Near Detector.

There are three DAQ modes required of the electronics. As described above, in Single Turn Extraction Mode, an event may occur in each RF bucket, for the $\sim 10 \mu\text{s}$ period of the spill. The second mode is to record cosmic rays during the interval of time between spills, which is approximately two seconds long. This is called Cosmic Ray Mode. These events happen less frequently, and will occur randomly in time with respect to the RF clock. The Near detector electronics must be capable of recording the events from the spill, while ensuring that there is adequate live time to record the cosmic ray events. The third mode of operation is an optional one, in the case that the accelerator uses Resonant Extraction instead of Single-Turn Extraction. In this case, the spill lasts approximately 1ms, and the rate of interactions is reduced. This is called Resonant Extraction Mode.

The requirements on the electronics for the Near Detector are quite stringent. The electronics must be capable of accurately measuring the charge from a photodetector that occurs from 1-2 photoelectrons. To accomplish this, the electronics should have enough resolution to resolve the charge from a single photoelectron above the noise floor of the electronics. An event from the beam might produce a shower, which can produce ~ 150 photoelectrons. In addition, there can be as much as a 3-to-1 gain variation in the pixels from the photodetectors. With all these factors, the electronics must have a dynamic range of 12-13 bits. As described above, the electronics must have low deadtime, and be capable of digitizing at the accelerator RF frequency of 53 MHz. To achieve this performance, the ASIC Design Group at Fermilab has developed a custom integrated circuit, which has been used in several applications to date. The device, called QIE, has been used by KTeV, CDF, and is being planned for CMS. The device can operate at 53 MHz, is pipelined so that there is no intrinsic deadtime, and has a dynamic range in excess of 16 bits. It is planned to modify this device to optimize it for the MINOS Near Detector front-end electronics.

The MINOS DAQ system is designed to be “triggerless,” in that there is no global trigger system. In Single-turn Extraction Mode, the system will digitize every channel on every RF clock cycle during the spill. The events will be timestamped according to the RF bucket with which they are associated. Data are transferred the front end crates to a VME readout board after the spill is over. The events will then be zero-suppressed before transferring the data to the back end electronics. A signal from the accelerator will inform the electronics when a spill is occurring.

In Cosmic Ray Mode, the electronics will operate somewhat differently. The system still digitizes at the RF frequency, but storage and readout will be triggered by a discriminated dynode signal from each PMT. When a cosmic ray event occurs, the signal from the dynode associated with that photodetector will fire the discriminator, and cause the readout of all channels associated with that photodetector, along with a timestamp. Zero-suppression will occur before transferring the data to the back end event builder. The primary difference between the two modes is that in Spill Mode, the dynode trigger is not used to initiate a readout.

In Resonant Extraction Mode, the electronics will use the dynode signal as a trigger during the spill. The electronics still digitizes continuously, but the dynode trigger will cause several RF buckets worth of data to be stored in a local memory, along with a timestamp. When the spill is over, the data are transferred tot the VME readout board.

6.3.2 System Requirements The following is a list of the general requirements on the electronics for the Near Detector:

1. Least Count Resolution

It is expected that the photodetectors will operate at a maximum gain of 10^6 . The worst-case pixel may be a factor or 3 lower, or 3.33×10^5 . The electronics must accurately measure the charge from a single photoelectron, with enough resolution to be above pedestal noise. A single photoelectron produces ~ 50 fC for the lowest-gain pixels. The least count resolution of the QIE is 7.5 fC. A single photoelectron would then register ~ 7 ADC counts above pedestal for the low-gain pixels. (We are exploring the possibility of modifying the QIE to have a least count resolution of 5 fC.)

2. Largest Signal and Dynamic Range

The largest signal from an event is expected to be ~ 25 mips. Each mip produces ~ 6 photoelectrons, which is equivalent to ~ 24 pC of charge for the highest gain pixels at 10^6 . This gives a minimum dynamic range of 3200, or 12 bits.

3. Digitization Rate

The system must be capable of digitizing at 53 MHz, the RF frequency of the Main Injector. In particular, the system must be capable of recording events that occur in successive RF buckets during the spill.

4. Deadtime

There must be no deadtime from the electronics during a spill. The electronics must be capable of measuring and recording all events which occur during the $\sim 10 \mu\text{s}$ spill duration.

For measuring cosmic rays, a live time of 80% is desirable. Cosmic rays will be recorded in the interval between spills.

5. Timestamping

All events shall be timestamped to a resolution of an RF bucket ($\sim 19 \text{ nS}$).

6. Zero-Suppression

All events shall be zero-suppressed. Only channel data above a programmable threshold shall be read out.

6.3.3 Description of QIE

The analog signal processing circuitry used in the front end electronics is based upon a custom integrated circuit developed at Fermilab called the QIE (Charge (Q) to Current (I) Encoder.) This device was originally designed for the SDC, and later adapted for the KTeV experiment at Fermilab [7, 8, 9]. It is fabricated in a $2 \mu\text{m}$, double metal, double poly process, and employs both CMOS and bipolar transistors.

The device is capable of continuous analog processing at 53 MHz without deadtime. This is accomplished by pipelining the analog operations inside the chip. The device has a wide dynamic range, and uses a "floating point" format to accomplish this. There are 8, binary-weighted, ranges in the device, and circuitry inside the QIE automatically chooses the "range of interest" for digitization. The 8 ranges are represented by 3 Range Bits, which are provided as an output from the QIE. The QIE puts out an analog voltage associated with the range of interest. An external flash ADC (FADC) performs the actual digitization. The combination of the two devices, operating at the same clock frequency, produces a continuous stream of digitized data without deadtime. If the ADC has 8 bits, then the total dynamic range of the combined devices is 16 bits (8 ADC bits, with 8 ranges.) The device has excellent noise and linearity characteristics, and is well matched for use with an 8-bit FADC. A block diagram of the QIE is shown in figure 6.3.

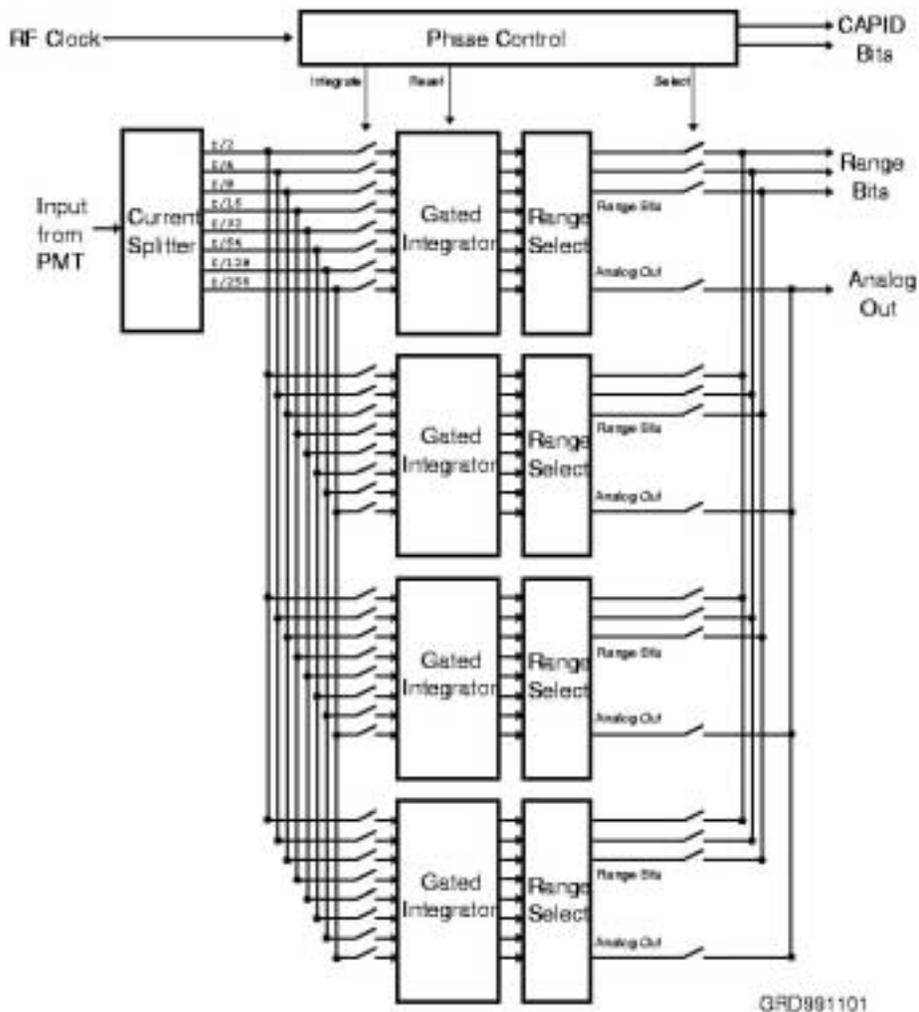


Figure 6.3 Block diagram of a QIE chip

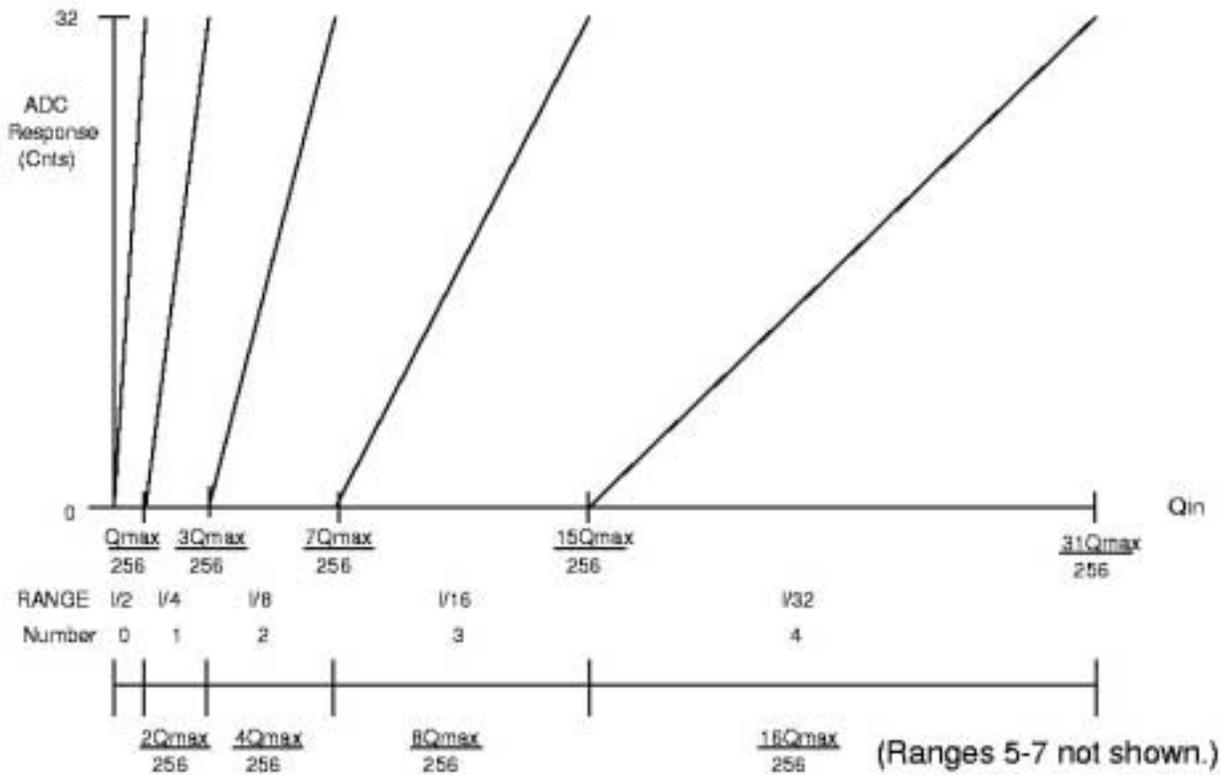
The QIE has four phases of operation. In the Integration Phase, the input current is split into binary-weighted fractions, which are then integrated on separate integrating capacitors. At the end of the integration period, the resulting voltages are held on the integrating capacitors for further processing. A buffer drives out the voltage from each capacitor to a set of comparators, which selects one of the voltages for digitization. This is called the Range Select Phase. The biasing is arranged such that one and only one of the ranges will be within the digitization range of the FADC. From this, a binary representation of the selected range is produced for output. Once a range has been selected for digitization, the Range Bits are presented on output pins, and the voltage on the corresponding integration capacitor is switched to the analog output of the device, making it available to the FADC for digitization. Allowing for settling, the FADC can be

clocked at the end of this clock cycle. This phase is called the Digitization Phase. After the FADC has digitized, the Range Bits are appended to the FADC bits to form the floating point data word. Next, all of the integrating capacitors are reset to prepare them for the next integration cycle. This is accomplished by closing then opening a switch around the integrating capacitor, which effectively shorts out the capacitor and removes the charge. This is called the Reset Phase.

Note that after the Integration Phase, it takes 3 additional clock cycles to process the signal acquired on the integration capacitors and prepare for the next integration cycle. Without additional circuitry, the device would be dead 75% of the time. To accomplish deadtimeless operation, there are actually 4 integrating capacitors on each of the current outputs from the splitter. Each capacitor on a range is part of an overall phase of operation for the device, i.e. while one set of capacitors (one from each range) is integrating, another set is being selected for range, another set is being digitized, and the other set is being reset. The phase of operation changes with each clock cycle in round-robin fashion. In order to keep track of second order effects, a two-bit identifier is appended to each data word, called the CAPID Bits. These bits identify the set of capacitors that were used to acquire and process a particular data word. This circuitry effectively pipelines the device, and produces deadtimeless operation. Thus, a QIE data word consists of 13 bits: 2 CAPID Bits, 3 Range Bits, and 8 FADC Bits.

Because the QIE uses a binary-weighted scheme to acquire and process charge signals, the transfer function for the device (plot of FADC bits produced versus input charge) has a unique shape. This is shown in figure 6.4. Each line segment represents the response of an integrating capacitor for a particular range. Note that this figure shows the response of one phase (i.e. always reading out the same CAPID.) There are actually 4 such plots for each QIE channel.

The principle behind the QIE is that the device always produces a digitized value which has ~0.4% (8 bit) accuracy over the entire range of operation. In order to “reconstruct” the amount of charge associated with the floating point number produced by the QIE, the QIE data word (FADC bits plus Range Bits) must be “linearized,” or turned back into a 16-bit linear number. This “unfolding” of the data are done by first carefully calibrating the QIE ranges, thereby obtaining a slope and offset for each range and for all phases, and then use a simple linear transformation to obtain the value of the charge.



QRD991101

Figure 6.4 Response function of a QIE chip. The effect of the different ranges can be seen.

6.3.4 System Architecture

There are two primary pieces to the system. The Front End Crates contains the QIE electronics. They are situated very close to the photodetectors, which is necessary in order to reduce noise associated with having long analog signal cables. Digitized data are held in FIFOs in the Front End Crates pending a readout cycle. When a readout cycle is initiated, the digitized data are sent to VME Readout Crates, which acts as a data funnel, collecting fragments of events together for further processing. The data are zero-suppressed and reformatted, and put into holding buffers, where it can be accessed by a VME computer, which resides in each crate. The computer collects data from all VME readout boards in the crate, time orders the data, and then sends it to the back end for event building and selection. The components of the system are described in the sections that follow. A block diagram showing how the parts fit together is shown in figure 6.5.

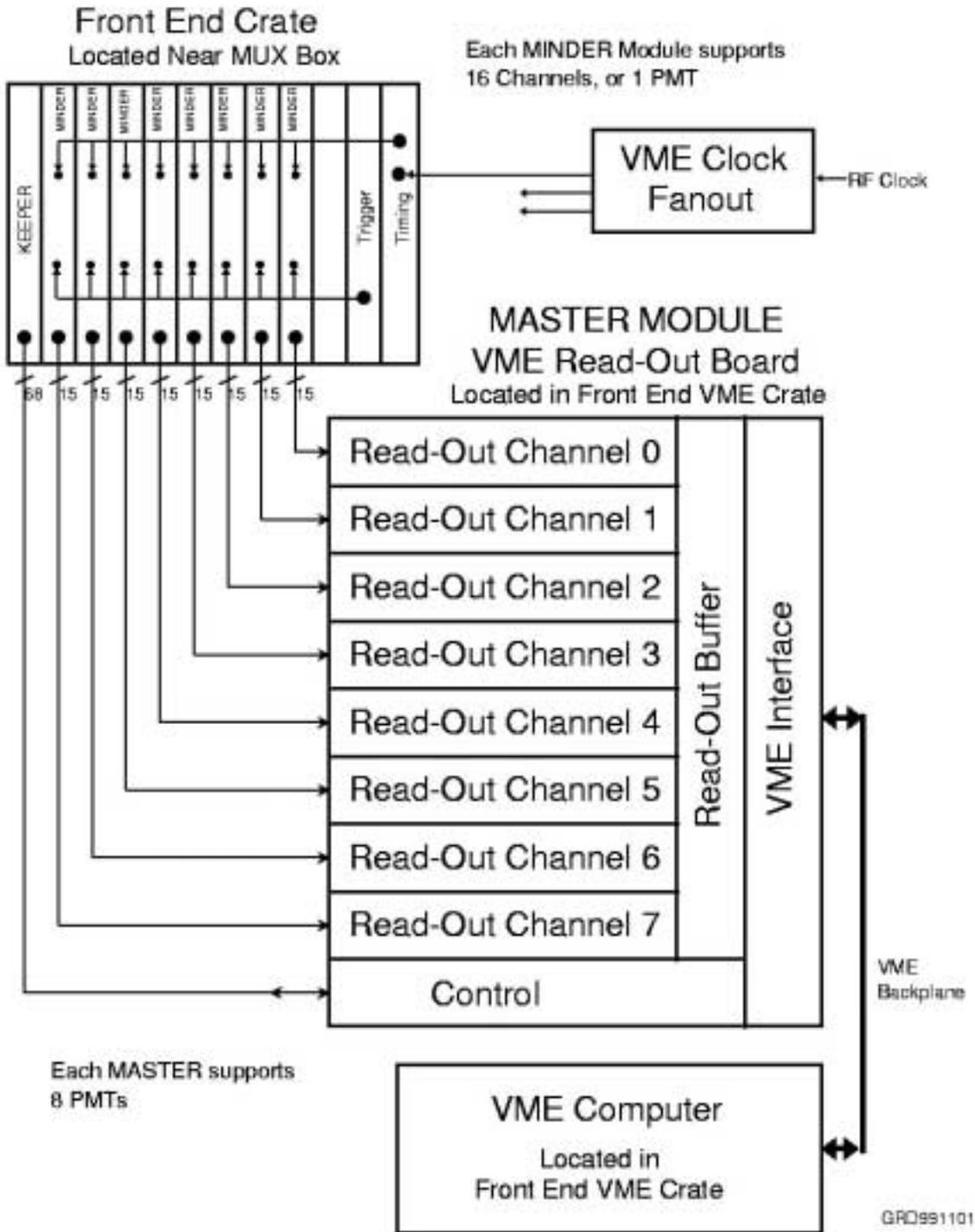


Figure 6.5 Schematic diagram of the near front end system architecture.

6.3.4.1 QIE Daughter Board

Each QIE is mounted on a small board. These are configured as daughter boards, which reside on a motherboard in the front end crate shown in figure 6.5. A block diagram of the functionality of the daughter board is shown in figure 6.6. The board contains the QIE, an 8-bit flash ADC, and a FIFO for storing the data. The board also contains circuitry for measuring source current, circuitry for injecting DC current into the QIE for performing electronics calibrations, and a current buffer.

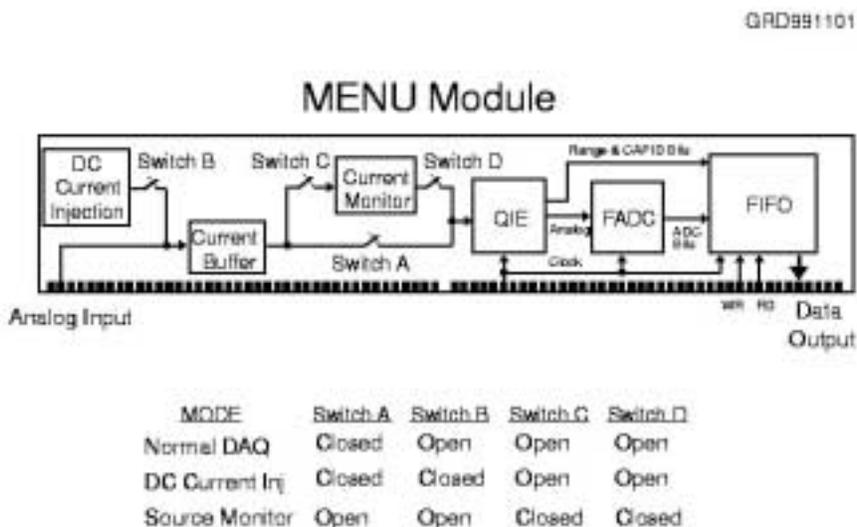


Figure 6.6 Schematic diagram of the near front end daughter board which contains the QIE chip.

A current buffer acts as a buffer between the QIE and the photodetector. The primary function is to accurately terminate the transmission line between the two, reducing the reflections that might otherwise occur from the fast edges of the photodetector signal. The QIE does not have a constant input impedance, and this buffer is required when the signal cables become long, as was the case in the implementation for CDF. For MINOS, the signal cables will be 1 meter or less, but given the short integration period of the RF clock, and also the requirement of measuring single photoelectrons, the current buffer is necessary to reduce the reflections as much as possible.

The QIE will be calibrated using a voltage-controlled DC current injector. It has been used successfully in CDF, to high precision. This circuitry will provide the means for obtaining slopes and offsets for all of the ranges and phases of the QIE, which are needed to linearize the QIE data. The DC current injector can also be used for diagnostic purposes.

The QIE and flash ADC are clocked continuously at 53 MHz. Data are gated into the FIFO depending on the mode of operation. These modes are described later. The FIFO is 1K words deep.

Data are read from the FIFO under control from the motherboard, which hosts the daughter boards, which is described in the next section. Due to limited space on the daughter boards, the FIFO cannot have simultaneous read/write capability, so the writing of data into the FIFO must be stopped during data readout. This creates deadtime, which is discussed later.

6.3.4.2 Front End Mother Board

The front end mother board contains 16 of the QIE daughter boards, which services one 16-channel photodetector. A block diagram is shown in figure 6.7.

The front end board has 3 primary functions: It handles the timestamping of data. It controls the multiplexing of data from the daughter boards to the VME readout board. And, it provides power, control, and interface functions for the operational support of the QIEs.

The timestamping is implemented on the motherboard using a 26-bit Grey-code counter, which counts RF clocks. This provides over 1 second of timestamping at the RF clock frequency. The counter is reset by a signal from the Clock System, and the counter value is incremented by the RF Clock signal. When a trigger occurs, the value of the counter is put into a FIFO, and becomes part of the header word that is sent to the VME readout board at the start of data transfer.

A “trigger” can occur in one of three ways. In Spill Mode, a signal is received from the Clock System, indicating that a spill is in progress. This causes the daughter board to continuously write data into the FIFO. The front end mother board holds off on transferring any data from the daughters boards until the spill is over, at which time the entire contents of all FIFOs are sent to the VME readout board. In Cosmic Ray Mode, a signal is received from the dynode trigger module, which resides in the front end crate, when there is an event of interest. This signal causes the data from several clock cycles to be written into the FIFOs. After the data are acquired, the front end sends this data to the VME Module. In the Resonant Extraction Mode, the dynode trigger causes the data from a fixed number of clock cycles to be written into the FIFO's during the spill. This is different from Single-Turn Extraction Mode, in which the data from every RF clock is stored during the spill. A timestamp is recorded from each trigger and these are stored in a Timestamp FIFO. When the data are sent to the VME readout board, the data are sent alternating timestamps and the data from the fixed number of clocks, until all data has been sent. In the fourth mode, the VME readout board can issue a trigger signal, for use in acquiring pedestals and calibrations. This signal can have a programmable duration, and is controlled by the VME readout board.

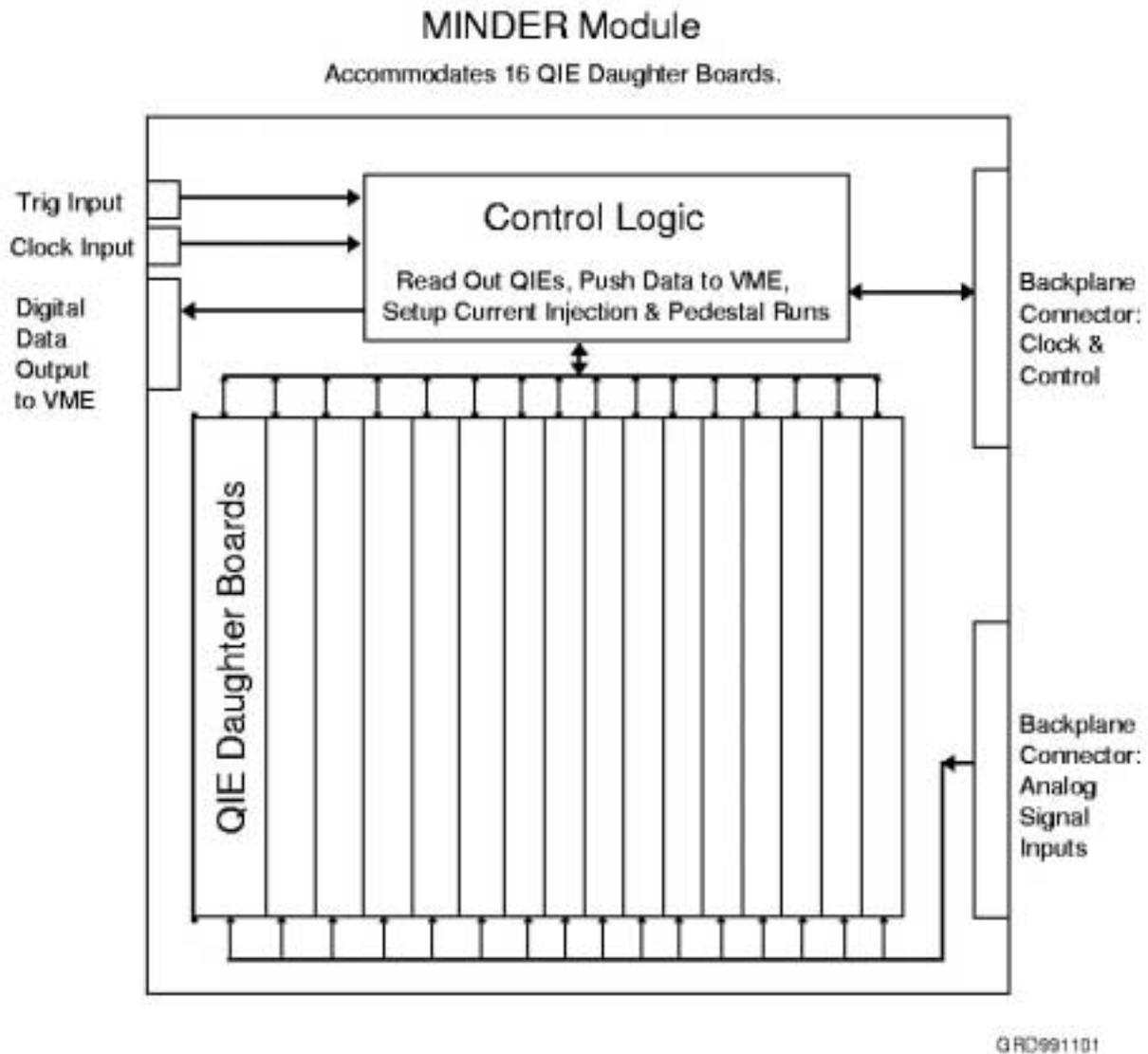


Figure 6.7 Schematic diagram of the near front end mother board. It holds 16 of the QIE daughter boards.

All of the FIFOs on the daughter boards operate synchronously, for all modes of operation. This means that when it is time to transfer data to the VME readout board, all FIFOs contain the same number of data words. (If they do not, then there has been an error, which will be detected.) When data are transferred to the VME readout board, the front end motherboard addresses the first data word in the first daughter board, then the first data word in the second daughter board, etc., until all 16 daughter boards have had one data word read from them. The front end motherboard then reads the second data word from each, then the third, etc., until all FIFOs are empty. In this way, the data format

and the readout scheme is the same for each mode of operation. The front end board sends data words to the VME readout board at 33 MHz.

In the different modes of operation, data are transferred to the VME Readout Board in the same way. The front end board is dead during this time. The deadtime is different for the different modes, because the amount of data that are transferred is different. When transferring data after a spill, the period that data acquisition is suspended is given by:

$$(10 \mu\text{S Spill} / 19 \text{ nS RF}) * (16 \text{ Channels}) * (33 \text{ nS/Word}) = \sim 275 \mu\text{S}$$

This deadtime occurs after the spill, so there is no loss of data during the spill. The time between spills is on the order of 1 second, so the deadtime is not an issue for the spill itself.

In Cosmic Ray Mode, the deadtime associated with sending data to the VME readout board is given by:

$$(8 \text{ data words/channel}) * (16 \text{ Channels}) * (33 \text{ nS/Word}) = \sim 4.5 \mu\text{S}$$

The maximum rate of signals in between spills (including noise hits, background radiation, and cosmic rays) is expected to be 1 kHz per phototube. The deadtime in reading out data from the dynode trigger is less than 1%.

6.3.4.3 VME Readout Board

The VME readout board serves as the interface between the back end system and the front end electronics. It resides in a 9U VME crate, which can be far from the photodetectors. It has three primary functions: It provides control signals to the front end Crate. It acts as a data funnel, receiving digitized data from the front ends. And, it processes the data received from the front end boards, preparing it for readout by the VME computer. The design is based on the SMXR used in the CDF Upgrade [10]. A readout board can service up to 8 front end motherboards, and each input channel can process data independently.

The data are pushed to the readout board by the front-end boards, and is written into a dual-port FIFO. The readout board reads the data as it comes in. The data from the front-end boards always come with the same format. The first two data words are header words. Then follows the QIE data, grouped 16 channels at a time. There is a special bit called the End of Record (EOR) which is asserted by the front end board, which informs the readout board when the end of data record has been reached.

The readout board first takes the two header words, which contain the timestamp, and converts the Grey-coded value into a binary value. The 16 QIE data words that follow

are associated with this timestamp. Any data over threshold in the first data set would get this timestamp. The next set of 16 words requires the timestamp to be incremented by one. The readout board counts data words, and increments the timestamp counter by one when a new data set is encountered (on every 16th word.) The counting of data words is also used to form a local channel ID.

As QIE data are read, it processed by the readout board. The first function is to convert the floating-point QIE data to a linear, 16-bit form. The readout board uses a look-up table (LUT) to accomplish this. The QIE data word (CAPID, Range Bits, and FADC Bits,) along with the running channel count, form an address into the LUT. The LUT is loaded with values in advance of data acquisition. The value in each location represents the linear, 16-bit data word associated with that QIE data word that points to it. The values are loaded by the VME computer, as a result of a calibration procedure. Each LUT handles the 16 channels associated with that input data channel (i.e. a front end motherboard.)

After the data are linearized, the readout board applies a digital threshold to the result. It passes those data that are over threshold, and applies the value of the running timestamp counter and a channel ID. The new data words are then put into one of two buffers, which can be accessed by the VME computer. One buffer is active for writing data making the other available for reading by the VME computer.

The Front End Crate has a simple controller. It is controlled by the readout board. A simple data link is provided between the readout board and the front end controller board. Through this link, the readout board can initiate DC Current calibrations, control DC current calibrations by writing to a DAC on the controller, enable radioactive source measurement circuitry, and initiate pedestal runs. These modes, in turn, are controlled by the VME computer, again by setting bits in a register on the readout board.

6.3.4.4 Interface to Back End and Trigger Farm

The interface to the back end electronics is provided by the VME computer, which resides in the 9U VME crate. The computer will operate under VxWorks, and is programmed to perform DAQ and calibrations. This computer can access registers on the readout board, which controls the acquisition of data, pedestals, and calibration data. The computer also controls the writing of data into the look-up tables on the readout board. The readout board is fully compliant with VME-64 protocol.

As data are acquired in the readout board, it is put into one of two buffers on the board. The timing system module in the crate controls which buffer is active for writing. This is done by using interrupts on the VME backplane. These also signal the the VME computer which buffer to read. The VME computer is then free to read out the contents of the inactive buffer. In this way, time blocks of data are formed, making it easier for the VME computer to time-order the data.

An important function of the VME computer is to process pedestals and calibration data, and to calculate the values to load into the look-up tables on the readout board. CDF used this technique, with a module very similar to the readout board.

To acquire pedestals, the VME computer can force the acquisition of data into the FIFOs on the daughter board by setting a bit in a register. The VME computer sets a bit in a control register on the readout board. This command is sent to the Front End Crate, which forces a “trigger” which acts in a similar way as Spill Mode. Data are collected in the FIFOs, and the front end mother board sends the data to the readout board. The readout board can be set up so that the raw data goes directly into the readout buffer. The VME computer can then access this data, and perform statistics on the data.

To perform DC current injection, the data acquisition sequence is similar. An additional step is to enable the DC current injection circuitry on the daughter board, and to write to a DAC on the front end control board. Data are acquired by the VME computer at each DAC setting. By sweeping the DAC through the range, the VME computer can acquire enough data on all of the QIE ranges to perform fits, thereby obtaining slope and offset for each range and phase, on every channel. The computer then uses these constants to calculate the linearized values associated with each QIE code, which are then loaded into the LUTs on the readout board. The LUTs have a flash memory, which saves the contents when power is removed from the board.

6.3.4.5 *Triggering*

A separate board is provided for triggering on cosmic rays. This board resides in the Front End Crate, and receives signals from all the dynodes of the photodetectors associated with that crate. The board contains discriminators with separate programmable thresholds. When a photodetector receives a signal from a cosmic ray, the discriminator for that channel fires, which is then used to trigger the acquisition of QIE data on the daughter boards.

In the simplest implementation, the signal from each discriminator is sent directly to the associated front end motherboard, which causes QIE data to be saved in the FIFOs on the daughter board. Each discriminator would have a point-to-point connection to the front end board. Other more sophisticated triggers are possible with this implementation, since all of the discriminators are on the same board. It is advantageous that they be off the front end boards, to reduce the possibility of noise pickup due to digital activity.

6.3.4.6 *System Timing*

There are two components to the Clock System on the Near Detector. The first is the Master Clock Module, which receives the RF clock from the Main Injector, and fans it out to every Front End Crate. The Master Clock provides two other signals. It broadcasts a reset for the timestamp counters on the front end mother boards, once per second. It

also sends out a signal indicating that a spill is in progress. Both of these signals must be timed precisely with the RF clock, to avoid timestamp problems in the front end modules. This module is similar to that built for the CDF and D0 Upgrades [11].

The second component is the Clock Fan-Out Module. This board resides in the Front End Crates. It receives the timing signals from the Master Clock, and in turn fans them out to each front end mother board. The fan-out will be implemented using point-to-point connections to reduce clock skew and other loading problems. This module is also similar to one built for CDF [11].