

# The MINOS High Voltage Controller

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The MINOS High Voltage (HV) Controller is a stand-alone C++ process which monitors and maintains operating potentials for the Hamamatsu M64 multi-cathode photomultiplier tubes. The text-based menu and interface to the LeCroy 1440-series hardware are presented here, including a detailed Command Manual. Implementation via the Intellution “iFix” Detector Control System Supervisor follows in a later document.

### I. OVERVIEW

The HV Controller is a custom-designed C++/Linux-based process. It operates several distributed LeCroy 1440 multichannel HV “Mainframes” via ethernet links to built-in RS-232 ports. Modelled after its MACRO (FORTRAN) predecessor [1], the MINOS implementation included not only a C++ rewrite but also a more sophisticated logical structure, required to coordinate control of four mainframes for each Far Detector Supermodule (as opposed to one each at MACRO). There are also two mainframes for the Near Detector, one “test” mainframe at the Soudan Underground Laboratory, and one at the CERN T11 test beam facility (twelve in all; see I).

In each Far Detector supermodule the lowest-numbered mainframe provides high voltage to the east side of the odd planes, the second to the east-side even planes, the third to the west-side odd planes, and the fourth to the west-side even planes (Table I). Odd planes correspond to the “*v*” electronics view, running diagonally from the lower east to the upper west, and even planes to the “*u*” view, running from the upper east to the lower west.

Each Far Detector supermodule includes 242 instrumented planes, 121 in each of the odd (*v*) and even (*u*) views. They are paired sequentially mod 2, or in odd-odd/even-even fashion. This produces 120 plane pairs (sixty odd and sixty even) and two unmatched planes. Each pair requires three M64 multi-cathode (sixteen channel) photomultiplier tubes on each side, with nine fibers passively multiplexed to each pixel. Unmatched planes use only two pmt’s each, one of which is only half occupied. This arrangement requires a total of  $120 \times 2 \times 3 + 2 \times 2 \times 2 = 728$  HV channels. The Near Detector and CERN T11 Test Beam systems are similarly organized but smaller in scale.

Each mainframe serves sixty full and one partially occupied mux boxes, or  $60 \times 3 + 1 \times 2 = 182$  active channels. The first 180 of these are arranged fifteen each on twelve sixteen-channel cards, yielding five single-sided plane pairs and one spare channel per card. For consistency the unmatched plane is serviced by a thirteenth HV card rather than with an *ad hoc* arrangement of spare channels. This underutilized card is an unavoidable but minor consequence of the fact that the number of planes is not divisible by twenty, but allows some flexibility in the event that changes are made in the system.

### II. THE LECROY 1440 HIGH VOLTAGE SYSTEM

The LeCroy [2] 1440-series high voltage system [3] is a “. . . multichannel, programmable high voltage system designed for large-scale applications where high reliability and performance are a necessity.” Although no longer manufactured (it was replaced by the 1450 series) the system is maintained by Fermilab Prep and several MINOS collaborators have experience with it.

**MINOS High Voltage Mainframe Schedule**

MF	Location	Planes	View	PC
1	Far	E-Odd	<i>v</i>	DCSHV1
2	Detector	E-Even	<i>u</i>	
3	(SM 1)	W-Odd	<i>v</i>	
4		W-Even	<i>u</i>	
5	Far	E-Odd	<i>v</i>	DCSHV2
6	Detector	W-Even	<i>u</i>	
7	(SM2)	E-Odd	<i>v</i>	
8		W-Even	<i>u</i>	
9	Near	E-All	<i>u/v</i>	DCSHV3
10	Detector	W-All	<i>u/v</i>	
11	CERN T11 Beam	All	<i>L/R</i>	DCSHV4
12	Test Stand	—	—	

TABLE I: HV Mainframe (MF) by location and service assignment. Odd planes correspond to the “*v*” electronics view, even to “*u*.” Near Detector mainframes service both even and odd planes, and a single LeCroy supplies both “*L*” and “*R*” views for the CERN T11 Test Beam apparatus.

The 1440 system is built around with a 1449 Mainframe, which holds a 1441 ( $\pm 15, +5.3$  VDC) Power Module and either a 1445 (13-bit “Economy”) or 1445A (16-bit “high performance”) Controller. In addition it includes one (1449E/ME) or two (1449M) 1 kW 1442 (+35.5 VDC) supplies, and up to sixteen high voltage cards (sixteen channel 1443NF/PF’s provide  $\pm 2500$  V, while eight-channel 1444NF/PF’s provide  $\pm 5600$  V, both with SHV connector outputs). While MINOS requirements could be satisfied by the low-power 1449E/ME we have selected the 1449M, in which the two 1442’s provide (+35.5 VDC) in parallel for up to eight 1443N cards each (0 to  $-2500$  V; Fig. 1).

Communications between the Linux processor and the LeCroy are provided by an ethernet card and four Intelligent Instruments EDAS 1025E-2 ethernet-to-serial interfaces (Fig. 2), located on each side of each supermodule. Each 1025-E2 has four ports, two of which provide access to the 1440 Mainframes via built-in RS-232 ports in the 1445A controller. The others are reserved for independent Detector Control System communications. RS232-compatible cables are shielded and limited to no greater than 1 m in length.

Various hardware settings allow the user to further customize 1440 operation. For MINOS, these have been selected as follows:

- **Baud Rate:** 9600 bd (maximum value). Set via jumper on the 1445A, header J6, placed in the highest position as indicated by the baud rates printed directly on the circuit board.
- **HV Ramp Rate:** 500 V/s (minimum value). Set via jumpers on the 1441, headers J10N/J11N/J12N (open/closed/open). The (unused) positive rates are set independently to the same value using J10P/J11P/J12P. Note that this serves as a backup to the much stricter software limit (section VI).
- **Voltage Program/Readback Scale:** 1 V/bit (minimum sensitivity). Set via jumpers on the 1441, headers J4/J5.<sup>1</sup>

<sup>1</sup>This configuration provides a theoretical maximum of 4096 V, but is limited by the 1443N to 2500 V (absolute value). Options range down to 0.375 V/bit with an upper limit of 1500 V, but make the code much less transparent. In addition individual channels fluctuate by  $\sim 5 - 10$  V from the requested voltage anyway, and 1500 V is not low enough to prevent damage to the M64 pmts should there be a catastrophic failure. The hardware HV limit is provided instead by the 1443 potentiometers (next item.)

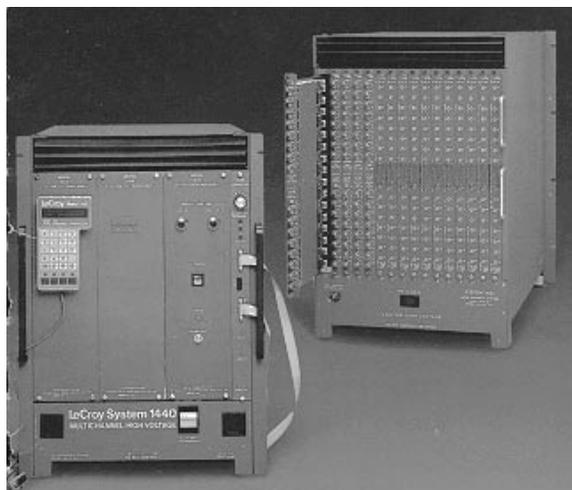


FIG. 1: The LeCroy 1440 high voltage system. The 1449 mainframe holds a 1554A controller (first narrow slot on right), a 1443  $\pm 15$ , +5 V Power Module (second, wider slot, with pots), and two 1442 +30.5 V DC supplies. The 1447 hand controller (upper left) is not used. Model 1443N high voltage cards provide sixteen channels of 0 to  $-2500$  V each (rear view).

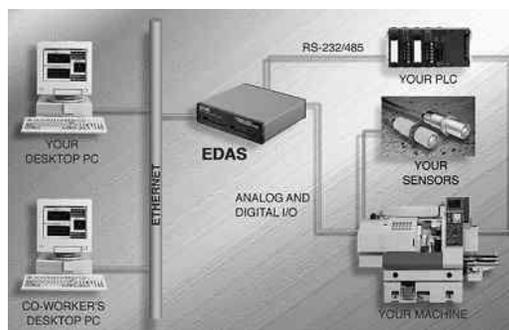


FIG. 2: The Intelligent Instruments 1025E-2 ethernet-to-serial interface (left) and communications cartoon (right).

- **Voltage Output Limit:** 1000 V (absolute value). To avoid accidental reset, ten-turn (lockable) potentiometers are replaced by fixed-value resistor networks. To accommodate a non-linear onset, the limit of 1000 V is set slightly higher than maximum operating potential of  $\approx 900$  V.

### III. LOGICAL ORGANIZATION AND LOCAL CHANNEL DATABASE

In each mainframe HV card slots are numbered from 0 to 15, with individual channels from 0 to 255. This “physical” or “hardware” channel assignment is mapped to a Logical Channel ID via the local HV database (nominally `hvsml.db`, `hvsm2.db`, `hvnear.db`, or `hvc1.db`) which is read at startup. In normal operation channels are tagged via both hardware and logical assignments, although changes in the physical channel numbers are transparent to the user. Some typical database entries are

* Label	MF/Cd/Ch	HV	PMT ser#	MUX ID, Ser#
*=====	=====	=====	=====	=====
1001-E0	1 00 00	-768	KA0566	EBM0-0 2014
1001-E1	1 00 01	-774	KA0528	EBM0-1 2014
1001-E2	1 00 02	-774	KA0767	EBM0-2 2014

1005-E0	1	00	03	-857	KA0696	EBM1-0	2008
1005-E1	1	00	04	-851	KA0751	EBM1-1	2008
1005-E2	1	00	05	-818	KA0815	EBM1-2	2008
1009-E0	1	00	06	-815	KA0834	EBM2-0	2002

The first character of the label indicates where the channel is located: the first or second Far Detector supermodule (“1” or “2”), the Near detector (“N”), or Calibration Detector (“C”). Test planes are indicated by (“T”). The next three digits give the plane number, and the two following the hyphen give the readout side (“E” or “W” in the Near and Far Detectors, “L” or “R” for the Calibration Detector and test planes) and pmt index (“0,” “1,” or “2”). The label is followed by a hardware channel assignment (LeCroy mainframe, card, and channel), default voltage, the M64 (pmt) serial number, and the mux box ID and serial number. The mux ID gives its location, and is repeated on the HV cable itself. In the Far Detector this is East or West side, Top or Bottom walkway, rack ID and box index.

Although records are typically grouped by mainframe for convenience, each is self-contained and they can be read in any order. Because planes are read out on both sides, however, the controller expects to associate six individual channels with each (three on each side, including test planes). During normal operation channels are selected by plane ID and all are run up and down together, reducing the potential for damage from stray light (when the mux box at one end is opened, light is transmitted to the other via the optical fibers).

Note that each mux box serves two planes, and that even and odd planes are served by separate LeCroy 1440 mainframes. Thus plane 1001 entries include both planes 1001 and 1003, served by mainframe 1 on the east and mainframe 3 on the west. Planes 1002/1004 are served by mainframes 2 (east) and 4 (west), so that the next plane in the mainframe 1 section of the database is plane 1005/1007 (see Table I).

Upper and lowercase characters are equivalent (the controller converts everything to uppercase), and comments and column headers are indicated by a leading “\*”, “#”, “!”, or “/”.

A single-mainframe (“expert debug”) mode allows access to individual channels in a single mux box, but “permanent” single channel needs for calibration or trigger electronics are addressed via “X” labels. These are “XSPR-01”, “XTRG-02”, *etc.*, for which the second through fourth characters are arbitrary and the last two are an index. Note that all “X”-type channels are be numbered globally; that is, “XSPR-01” and “XTRG-01” are indistinguishable (attempted simultaneous use will generate a warning).

#### IV. COMMUNICATIONS DATABASE

A short mainframe hardware link database (nominally `hvc.com.db`) is also read out at startup. It contains one record for each mainframe, which for the first supermodule is

```
*ID Label Device
*== =====
1 SM1E-ODD 198.124.213.68:0
2 SM1E-EVN 198.124.213.68:1
3 SM1W-ODD 198.124.213.69:0
4 SM1W-EVN 198.124.213.69:1
```

This gives the IP address of the EDAS 1025E-2 ethernet-to-serial interface and the port number (0 – 3). Device names like `/dev/ttyS0` (COM1) and `/dev/ttyS1` (COM2) indicate direct links via PC parallel ports, utilized by the Calibration Detector and Test Mainframe.

## V. CONTROLLER ORGANIZATION

The controller itself consists of approximately 2500 lines of C++ code, ported from the MACRO (FORTRAN) version and adapted for MINOS in a unix (Linux) environment. The entire Far Detector could in principle be overseen by a single HV process, but it was not considered desirable to span supermodules so there is a separate process for each. These are coordinated by the DCS Supervisor, an Intellution iFix package (section VII). The HV processors also provide local detector-side access to the high voltage and other DCS systems.

The controller is a text-menu interface, which is typically inactive. That is, overall control is provided by the user, and the controller will not monitor voltages or perform other operations unless specifically requested. It does not, furthermore, interpret the results of its operations beyond the production of text output.

In “local” mode (the default) the controller accepts and writes to the default I/O device, and is nominally terminated after the required tasks have been accomplished. In remote mode (initiated via `hv -r`) the controller opens a virtual port (1060) through which it can communicate with the iFix Supervisor or another user via telnet/ssh. In this mode the controller process remains in memory but lies dormant until it receives specific requests from the iFix DCS Supervisor (Section VII).

## VI. HV COMMAND REFERENCE

Whether operating in local or remote mode, upon startup the controller reads the communication and channel databases, checks the status of each known mainframe, and awaits commands. These are available interactively through the HELP command with individual commands via `HELP {command}`. At the present this produces the following output:

READ (abbr R): Reads active HV channels. Flags voltage errors. Report voltages for all known active channels (see SELECT). Two kinds of errors are flagged: DEFAULT errors, in which the requested voltage is not equal to the default (“!”), and READBACK errors, in which the readback is not equal to the requested voltage (“\*”). Thus a typical READ response will include lines such as

Label	MF/Cd/Ch	PMT ser	MUX ID, ser#	Default	Request	Actual
=====	=====	=====	=====	=====	=====	=====
1009-E0	1 0 6	KA0834	EBM2-0 2002	-815	-815	-813
1009-E1	1 0 7	KA0686	EBM2-1 2002	-815	-815	-815
1009-E2	1 0 8	KA0989	EBM2-2 2002	-818	-818	-818
1013-E0	1 0 9	KA0837	EBM3-0 2010	-898	0	0 !
1013-E1	1 0 10	KA0442	EBM3-1 2010	-755	-755	-775
1013-E2	1 0 11	KA0494	EBM3-2 2010	-787	-787	-790 !
1017-E0	1 0 12	KA0548	EBM4-0 2017	-841	-841	-830 !*
1017-E1	1 0 13	KA0821	EBM4-1 2017	-843	-843	-842 !
1017-E2	1 0 14	KA0824	EBM4-2 2017	-843	-843	-844 !
XSPR-01	1 0 15	.....	.....	0	0	-22

At the present time default errors are generated for any value except that in the database, and readback errors are generated for voltage differentials equal to or greater than ten volts. To accommodate the tendency for “zeroed” channels to float when nearby channels are active, however, a higher threshold of sixty-four volts is applied when the request is zero. Note that the readout provides both the physical and logical

channel tags, as well as the location of the mux box (also printed on the HV cable). Errors also produce an audible warning bell (ASCII “\a”). Readout of an entire supermodule requires two to three minutes.

SET (no abbr): Sets active HV to default values. Employs slow ramp to guard against HV overshoot.

Voltages are approached in a binary-step (logarithmic) sequence, with typically five to six cycles required to reach full potential. The entire process may require up to ten minutes for a full supermodule.

ZERO (abbr Z): Zero all channels (active or not) in all mainframes. The zero is immediate and includes *all* channels, active or not, including test, spare, and other “X”-type labels, as well as unused (unmapped) channels.

SELECT/ADD (abbr SEL/ADD): Select active planes for subsequent READ/SET commands. Range can be provided on command line. Use hyphens for inclusive range, ADD to merge with existing range, ALL for all planes, and ALL! to include Xxxx and Tnnn. NONE deselects all channels. In single mainframe mode, select by LeCroy channel number rather than plane.// Allows the user to select individual planes for subsequent READ, SET, *etc.* operations. Because multiplexing spans even-even and odd-odd plane pairs, the basic SELECT unit is two mux boxes, which handle opposite sides of the pair. In normal mode SELECT will not address individual channels within a mux box, nor will it enable one side of a plane without the other. These can be selected in single mainframe mode, using their physical channel number rather than logical (plane) label.

STATUS/ENABLE/DISABLE (abbr ST/EN/DIS): STATUS returns HV interlock and global HV status. ENABLE/DISABLE (ON/OFF) sets HV to zero and enables/disables HV output.// STATUS reports whether each HV mainframe is enabled and whether its global error bit is set. This occurs when any one of the readback voltages differs from request by more than 64 ADC counts (64 V in the current operating configuration). Status is called automatically on startup. Note also that mainframes are ZEROed before each ENABLE or DISABLE command.

LIMIT (abbr L): Measures/sets global single-channel current limit.// A single register holds the global single-channel current limit for for each mainframe. In the current configuration this is nominally set to  $-100\ \mu\text{A}$  per channel (approximately 1 mW), but it can range from 0 to  $-255\ \mu\text{A}$ . Channels which would require more than the allowed current will not reach requested potential and will (nominally) produce a channel error in STATUS. Loss of power usually resets the current limit to its maximum value.

CLEAR (abbr CL) Clear read buffer and mainframe faults.// CLEAR is called automatically upon startup and each time a new mainframe is addressed. In practice fault conditions generally indicate errors which cannot be addressed by repetition of this command, but for completeness it is included anyway as a voluntary call.

NEW/RENEW (abbr NEW/REN): Read new default voltage map from user-specified file, or renew/refresh existing map.// Allows the user to reset the channel database, or input a new database for testing or calibration purposes.

MAINFRAME (abbr M, MF): With argument, select a single LeCroy 1440 mainframe. Without argument, reselect all available mainframes.// Enters single-mainframe “expert debug” mode. Primarily, allows access to normally unmapped channels (see DUMP) and individual channels within a particular mux box. In single-mainframe mode these are selected by physical channel number rather than logical ID (see SELECT).

DUMP (abbr DUM): Read ALL channels, mapped or not. Single mainframe mode only.// When a single mainframe is selected, searches for empty slots and prompts for readout of all physical channels (regardless of whether they are in the channel database or not).

MANUAL (abbr MAN): Manually set default voltages, channel-by-channel. Single mainframe mode only. Prompts to SET new values.// When single mainframe mode is selected, allows the user to manually set default voltages, channel by channel. Prompts for immediate set to these new defaults, which remain in effect until a future use of MANUAL or RENEW.

VERBOSE (abbr VER): Toggle verbose mode. In single mainframe mode, will also explicitly transmit any argument string.// Dumps serial communications and other debugging information to the standard output. In single mainframe mode, also transmits *verbatim* any argument string to the LeCroy controller. WARNING: can produce copious output, and no safety or syntax checks are made on the argument.

EXIT/QUIT (abbr: E/Q/X/K): Close all I/O devices and files, terminate program. X exits (ungracefully) without closing anything. Kill also terminates remote server, if active.// Exit/Quit and Kill are identical in local mode, while the latter is required to explicitly terminate the HV controller as well as the current connection (this does not guarantee, however, that the server will not exit anyway via E/Q). The X option should function identically to E/Q in normal operation, but will not explicitly kill the remote server nor close sockets and other links.

## VII. THE DCS SUPERVISOR AND MINOS DATABASE

In normal operation the HV controller is called by the DCS Supervisor, an Intellution iFix process. Communications are provided by Berkeley sockets, which will allow the Supervisor to request (automatic) periodic HV readout, as well as asynchronous (user-direct) commands READ, ZERO, SET, *etc.*. A “debug” option opens a direct text-based link to the controller for more detailed HV operation. In order to avoid duplication of the entire HV record, the channel map and operating potentials are dumped to a text file and passed directly to the MINOS (Oracle) database. The iFix supervisor retains and flags only error records, including time stamp, channel tags, and error condition.

## VIII. STATUS

As of this report, the HV controller code has been in successful operation for approximately six months at the Calibration Detector site (the CERN T11 test beam facility), and four months at the Far Detector. Future hardware installation will include the second Far Detector Supermodule in September/October 2002, followed by the Near Detector.

Although the software system is complete as installed, modifications and upgrades will continue for the life of the experiment. Primarily this includes implementation of the iFix and database links, but other changes are planned:

- Implement iFix Supervisor -directed operations (already tested, but not fully detailed).
- Implement HV/Oracle Database link (only preliminary theoretical model exists).

- Replace pre-beta release at the CERN Calibration Detector (originally expected to occur automatically as the initial installation failed to satisfy experimental needs, but as this has not occurred we are planning a dedicated trip contemporaneously with the next UK Collaboration Meeting).
- Continued field testing of single Mainframe (MF) and MANUAL (debug) modes, including new C++ code and/or scripts for light-leak testing and other “special operations” sequences.
- Modify DUMP to survey HV card slots before readout (*i.e.*, read only slots with cards in them).
- Continued field testing of error thresholds. Test “terminators” for unused HV channels to prevent “float.”
- Explore multiple-channel READ access, to determine whether speed of current single-channel organization can be improved. That is, determine whether the readback rate is determined primarily by HV “settling” time, ASCII data rate, or channel addressing time, and adapt the program accordingly.
- Implement automatic current limit verification during startup STATUS call, to correct limits reset by AC power failure or other hardware failure.

Although this list contains several items, none are nominally very involved. We are scheduling a two-three day HV upgrade for January 2001 in which the most straightforward will be addressed, and plans can be made to treat those issues which prove more intractable.

#### REFERENCES

- [1] M. Ambrosio *et al.*, *Phys. Rev. D* **56**, 1407 (1997); **56**, 1418 (1997).
- [2] <http://www.lecroy.com>.
- [3] <http://www-esd.fnal.gov/esd/catalog/main/lcrynim/1440.htm>.