

Specifications for the MINOS Near Detector QIE

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0. GENERAL DISCUSSION

This discussion is based on the assumption that the MINOS QIE will be a modified QIE5b6. Details not specified are left to the IC designer.

The integration capacitors of the QIE5b6 are 1 pF, but our desired 2.5 fC per count sensitivity (with an 8-bit ADC) would be more naturally achieved with smaller capacitors, closer to 0.3 pF. However, we are advised that parasitic effects would then be predominant, resulting in greater voltage dependencies, process variations, etc.

To achieve 2.5 fC per count sensitivity with capacitors larger than 0.3 pC, we would operate the chip with a reduced Capacitor_Reset_Voltage_Range (CRVR), which would reduce the output voltage swing proportionally. For example, with 1 pF capacitors we would want to reduce CRVR (normally 1 volt) to 0.3 volts, resulting in a 0.3 volt output swing. An extra gain factor of 3.3 would then be applied externally. Among the possible disadvantages of this might be increased noise, and increased variations in the switching points of the various current ranges (relative to the output swing). The latter would result in our having to map the QIE output into a smaller fraction of the ADC input range in order to guarantee successful digitization.

We rely on the IC designer's judgement about the best compromise between capacitor reduction and CRVR reduction.

Because the detector pulses will often overlap two clock periods, it is thought to be important that the charge loss compensation features of the QIE5b6 be kept.

In the Near Detector, we do not expect to observe signals greater than about 24 pC. An eight range QIE with the specified resolution will handle much larger charges, so the full scale input listed below is not a specification, but just a statement that the QIE full scale will be sufficient for the Near Detector.

We imagine there might be two prototype submissions during year 2000, and we want to set the following schedule goals.

1st prototype submission:	January, 2000
Receive prototype and test:	March – May, 2000
2nd prototype submission:	June, 2000

Receive prototype and test:	September – November, 2000
Production submission:	December, 2000
Production chip delivered:	March, 2001

1. ANALOG INPUT

Lowest range resolution: 2.5 fC per count, +/- 30%, with an 8-bit ADC.

Full scale input charge: (Not specified, except that it should be at least 24 pC.)

Max. instantaneous current: 10 mA.

Quiescent voltage: +1 volt, nominal.

Impedance: 200 ohms, maximum.

2. ANALOG OUTPUT

Mode: Differential.

Differential output swing: 0.3 volts, minimum. (1.0 volts, preferred.)

Common mode voltage: (Not specified. This is expected to be +5 to +6 volts, but a lower value, such as 2.5 volts, is preferable.)

Output settling: Driving a 10 pF load (in addition to the QIE chip and its bonds), the output should settle sufficiently within 15 nsec after the corresponding clock edge that the other specifications are met.

Output droop rate: 0.5 volts per microsecond, maximum.

Equivalent noise charge: 3 fC maximum, with a source capacitance of 300pF.

Range switching: For every range of every phase, and for every device, the difference between the highest and the lowest output voltages (differences) of a given range should not exceed 110% of nominal, nor be less than 85% of nominal.

3. DIGITAL I/O

Inputs:	CLOCK and RESET.
Input mode:	True differential.
Input levels:	LVDS. Differential voltage swing is approximately 350 mV. Differential skew is expected to be 500 picoseconds, or less
CLOCK frequency:	53.1 MHz.
RESET operation:	Should be completed within one clock cycle after assertion. Timing should not be critical, that is, the RESET operation should succeed so long as RESET overlaps the period during which CLOCK is (say) high.
Outputs:	3 RANGE bits, 2 PHASE bits.
Output levels:	Should be able to drive TTL or low voltage TTL devices. IC designer is asked to decide whether these are differential or single-ended, voltage mode or current mode (into external termination resistors).
Output settling:	With a 10 pF load (in addition to the QIE chip and its bonds), the digital output settling should be such that it is possible to identify a period of at least 10 nanoseconds duration during which the digital outputs of all produced devices are simultaneously valid. The position of this interval should be stable against temperature changes.

4. LINEARITY AND STABILITY

Linearity:	The linearity of each of the 32 response ranges should be such that a linear least-squares fit of any range, with 5 equally-spaced measurement points, will allow the input charge to be reconstructed to within 1% of itself or 7 fC, whichever is greater.
Temperature stability:	The reconstructed input charge should not vary with temperature by more than 1% per two degrees C., or 7 fC per two degrees C., whichever is greater.

Time stability: The reconstructed input charge should not vary by more than the greater of either 1% or 7 fC in any four hour period, when temperature and power supply levels are held constant.

Power supply dependence: (Not specified. IC Designer is asked to specify how much power supply regulation will be required to meet the rest of these specifications.)

5. POWER SUPPLIES

Voltages: Positive supply voltages and ground. Exact levels to be determined by IC designer.

Power consumption: (Not specified, but more than 0.75 watts begins to pose a heat removal problem in the experimental hall.)

6. OPERATING ENVIRONMENT

Temperature range: 20 degrees C. to 55 degrees C.