

**Note on VA Readout of M16 Photomultipliers
for the MINOS Experiment
(with Appendix for Conceptual
Design Review, Oct 1 1999)**

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1. General

We describe a proposed readout which is based on the VA chip series from IDE Corp. (Oslo, Norway). This chip provides a charge sensitive preamplifier, a shaper, sample/hold for each channel and is followed by an analog output multiplexer as shown in Fig. 1. The VA chip series was originally designed and used for silicon detectors with the per channel circuitry constructed on 42 micron pitch to match the 50 micron pitch of a typical silicon detector. Versions have been constructed with 128, 64, and 32 channels per chip. The chip has also found use in non-silicon applications such as cathode pad readout in the Cleo3 RICH detector. Hamamatsu is currently developing a PMT base using the VA chip as well.

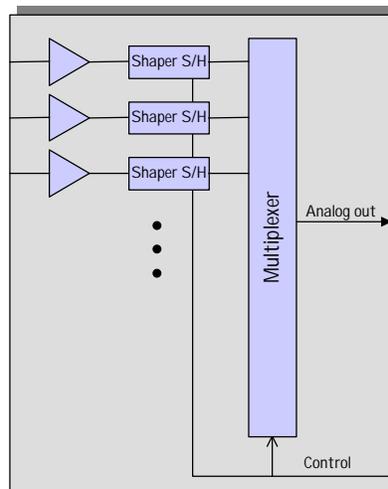


Figure 1 - VA Chip Architecture (IDE Corp Oslo, No.)

Typically, IDE markets this device by tailoring features to customer needs. Features which are easily adjusted are gain (preamp feedback capacitor), shaping time, and number of channels. The ideal match to an M16 PMT is a 16 channel device. Since a 32 channel VA chip is already quite small, there is no financial incentive to produce a 16 channel version and so we propose to use the VA32 with half of the chips channels unused.

2. Signal size and dynamic range requirements

2.1. Anode signals

PMT gain is considerably higher than required for compatibility with VA chip. For the moment, we assume that PMTs will operate at nominal gain $1e6$ with the low gain pixels operating at no less than 33% of nominal. The maximum signal is taken as 150 photoelectrons which gives us the following;

$$\begin{aligned}Q_{\max} &= 150 * 1e6 \text{ electrons} = 24 \text{ pc} \\Q_{\min} &= 33\% * 1e6 \text{ electrons} = 53 \text{ fc}\end{aligned}$$

Thus ratio $Q_{\max}/Q_{\min} = 450$ (9 bits) . Since we require high efficiency at recognizing single photoelectrons, we demand significantly higher system dynamic range ~ 13 bits.

When used with PMTs operating at high gain, we do not expect noise levels in the VA preamplifier (integrator) to dominate its dynamic range. Noise calculations for the VA result in enc well below 1 fc. VA noise is expected to be dominated by voltage statistics on its sample / hold capacitor. This is given by;

$$\sqrt{kT/C} \approx 100 \text{mV}$$

With the VA's largest signal capability of order 1 Volt, this gives an effective maximum dynamic range of $\sim 1e4$ or 14 bits. IDE estimates maximum dynamic range to be ~ 13 bits.

2.2. Dynode signals

If we assume single dynode gain to be 2 – 4, then minimum single photoelectron dynode signal will be ~ 25 fc. A variety of choices exist for amplifying and discriminating these pulses. An equivalent noise charge level of well under 1 fc is not difficult with shaping times of order 15ns. Various configurations of discriminator can be used for this purpose as well as a number of wire chamber ASDs now available. These are not described in this note.

3. Basic Architecture

3.1. Front End Boards (FEB)

The readout we propose is based on a general architecture shown below in Fig. 2.

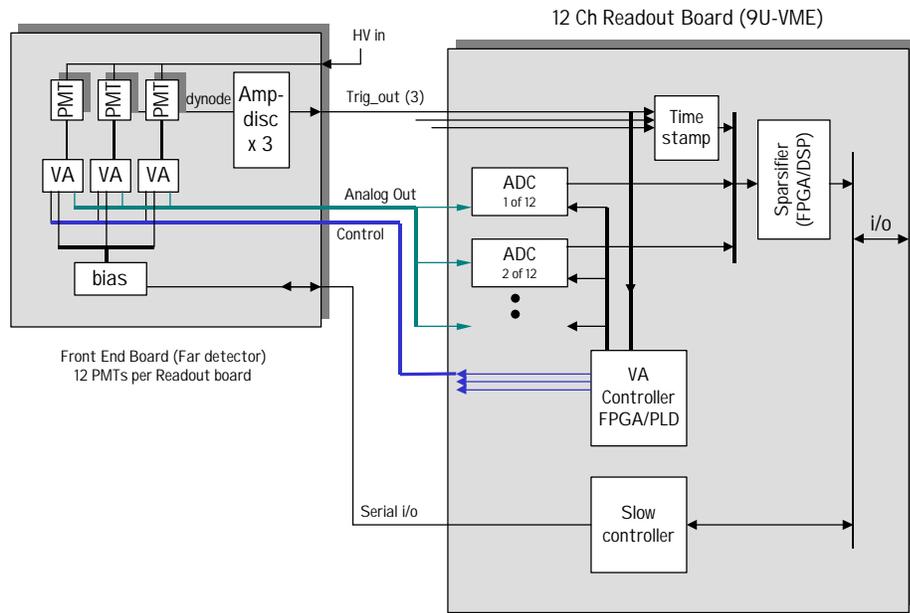


Figure 2 - Basic VA Readout

In this scheme, each Mux-Box is associated with a Front End Board which is mounted onto it in a separate shielding enclosure. The three PMTs of the Mux-Box are physically decoupled from the FEB as shown in Fig. 3.

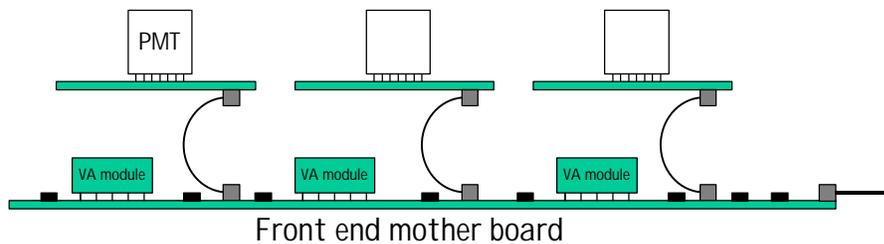


Figure 3 - Front End Board (FEB)

The PMT bases are connected to the FEB by a short ribbon cable thus allowing independent optical alignment. Front end electronics is thus kept out of the Mux-Box, which must be independently light tight. In this scheme, triggering is done using the PMT dynode signal and is, thus, not generated on an individual pixel basis. Each dynode trigger will be generated by an amplifier/shaper/discriminator with peaking time of order 15ns.

3.2. Readout Boards

ADCs are located on Readout Boards which are located in mini-crates distributed along the detector. Their size and location is dictated by cable length considerations. The Readout Boards receive the triggers from the FEBs and pass them to a controller FPGA. The controller contains state machines for each ADC channel and are responsible for toggling out the analog data from the VA chip and controlling the ADC. Each trigger results in the readout of all 16 active channels in the VA chip at a rate of 150 ns – 200 ns per channel. The readout time for 16 channels is the total of the shaper peaking time (0.5 - 1 us), readout time of the analog multiplexer (~ 3 us), and some recovery time after the readout during which the preamp and shaper levels settle back to pedestal (~ 2 us) . We thus estimate the total readout time to be ~ 6 us.

After VA readout, the ADC data are stored in fifos and processed by the Sparsifier (FPGA or DSP). The Sparsifier subtracts pedestals from each channel and passes on non-zero data for VME readout. Pedestal runs are recommended at intervals of approximately one per day and data are stored in on-board memory available to the Sparsifier. This is a typical architecture for VA readout of which numerous examples exist.

3.3. Cabling

3.3.1. Digital signals

For reasons of minimizing radiated interference from digital signals, these will be transmitted using the LVDS (Low Voltage Differential Signal). The signals to be transmitted are the VA control signals of which there are about a half dozen, the dynode trigger signals, and the Slow Control signals. Digital cables will be flat ribbon cable on 0.025” pitch.

3.3.2. Analog signals

The VA multiplexer output is a differential current which must be driven via twisted pair shielded cable to the Readout Board. There is a potential limitation to the length of this cable due to cable losses and dispersion. Dispersion manifests itself in a long low level tail in the return to baseline after a large pulse. Measurements of this were done using various lengths of cable of solid dielectric (RG174) and foam dielectric types (RG58A). These cable types are not differential but were used to indicate the effects of dispersion. The results are shown below in Fig 4

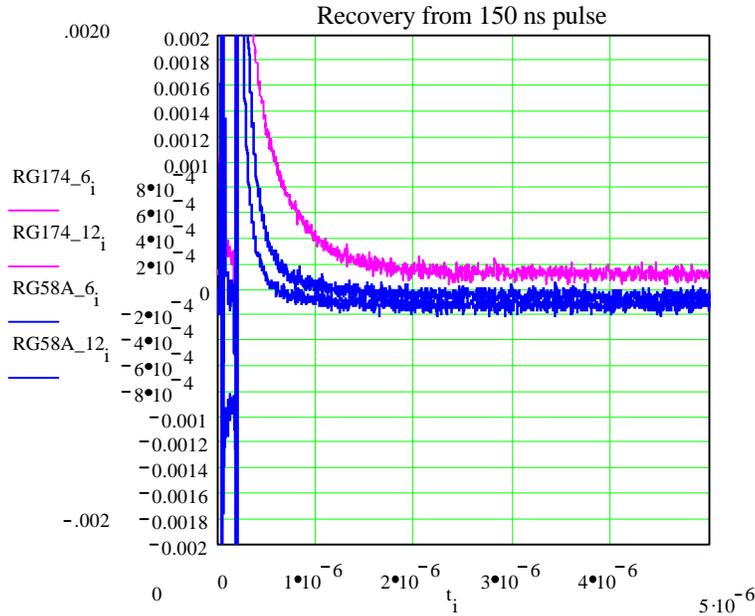


Figure 4 - Tail due to cable dispersion

The top traces correspond to 6' and 12' lengths of solid dielectric cable while the lower (blue) traces are for expanded dielectrics. In the latter case, residual signals of order $1e-3$ are seen in adjacent mux time slices. Return to baseline at the $1e-4$ level, required of a 14 bit system, occurs within a microsecond. The effects are small and can be calibrated out off-line. The cable we propose to use is 16' expanded ptfе to minimize this effect.

4. Far detector readout

Rates in the far detector are dominated by PMT single photoelectrons. We assume a worst case rate of ~ 1 kHz per phototube. If we assign one ADC channel to each VA chip, as indicated in the basic readout scheme of Fig. 2, the total demand we are placing on the ADC is exceedingly low; the product of PMT trigger rate and VA readout time.

$$6\mu\text{s} * 1\text{kHz} = 0.6\%$$

Given this low demand, it makes far more sense to utilize one ADC channel for each Front End Board containing 3 VAs instead of one per ADC. This scheme is shown in Fig. 5. Since during a VA readout cycle, the remaining two VA chips are capable of storing a new incoming signal, there is no additional deadtime incurred in this scheme. A trigger on ch-2, for example, is not lost if the ADC is busy processing ch-1. The sample/hold of VA-2 is activated and the signal remains stored until the ADC is free to process it. Thus, the ADC utilization is 1.8% while the “deadtime” for

each PMT remains at 0.6%. This results in a very compact readout with one Readout Board servicing 36 PMTs.

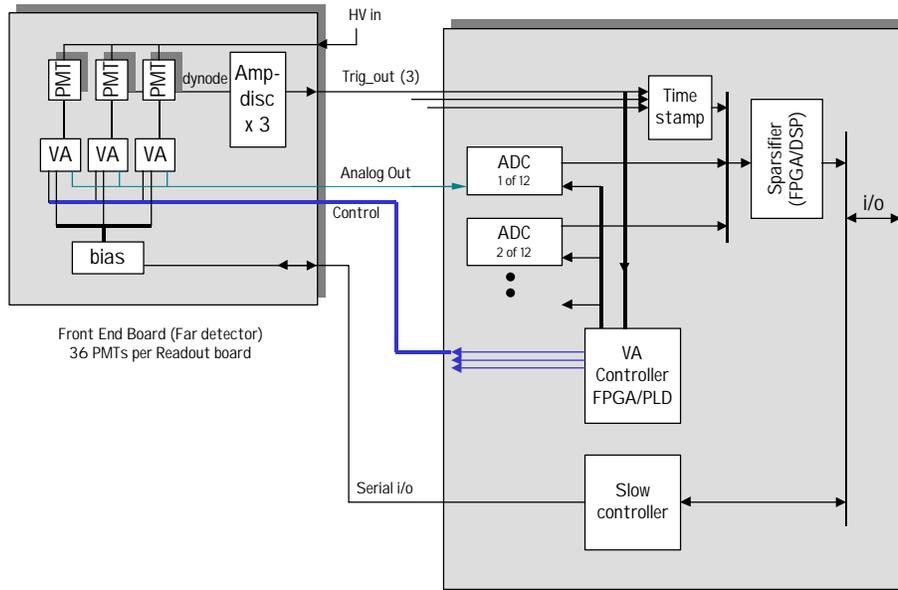


Figure 5 - Far Detector Readout

There is some additional complexity in utilizing a single Readout Board for twelve FEBs. One issue is cabling. Each Readout board must receive twelve digital and twelve analog cables. A single width 9U VME board does not have enough panel space for this and so the cabling must be divided between the Readout card and a simple mezzanine card which is attached to it. The VA controller must also be more complex than in the basic scheme. The controller contains one independent state machine for each front end board. This state machine keeps track of its three VAs in the manner described. This can be accommodated using high density and high pin count FPGAs or CPLDs.

5. Near Detector Readout

5.1. Rates

Readout rates in the near detector are such that use of a single VA chip per photomultiplier would result in excessive dead time. We propose use of multiple VAs per PMT in this region. The idea is that each PMT pixel anode is tied to two or more VA chip inputs which are capacitively coupled using a network shown in Fig. Xxx. In this configuration, charge divides in proportion to the ratio of capacitor C_0 to the total node capacitance. This offers the opportunity to divide charge between VA channels as well as to achieve overall attenuation. The latter is one means of accommodating the large PMT signals without the need of a large integrator feedback capacitor. It

should be noted that IDE has tested this configuration with several channels within a chip and verified that it works as expected.

A detailed discussion of rates and deadtime is found in section 6.

5.2. Near Detector Readout Board

The architecture for the near detector is shown below in Fig. 6

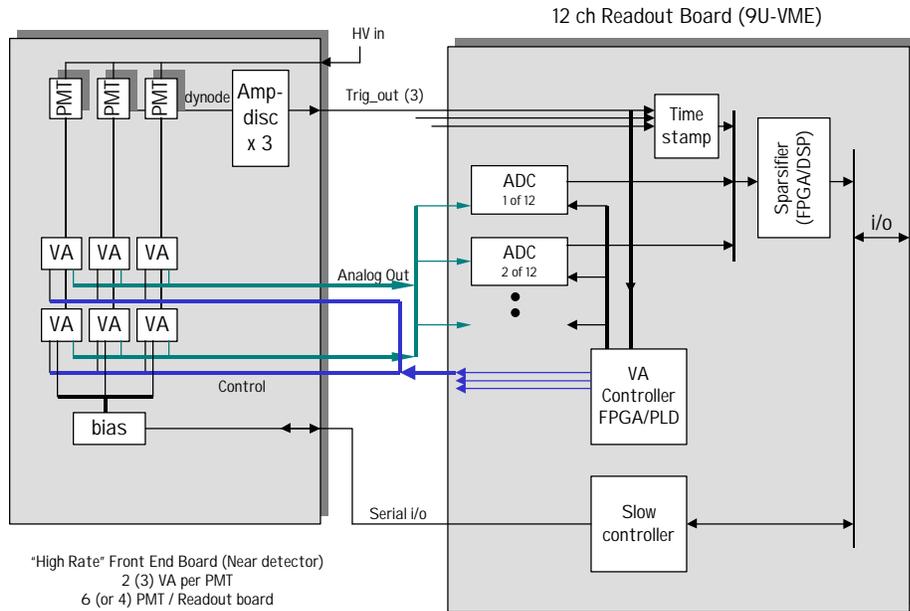


Figure 6 - Near Detector Readout

6. Deadtime Issues

6.1. Statistics

It is necessary to use queuing theory formulas to calculate the deadtime correctly. (Pure Poisson statistics overestimates the deadtime because it does not take into account that a rejected event does not take any processor time.) Our problems are known in queuing theory jargon to be of the form $M/G/c/c$. The formula for the loss rate in these cases was derived by A. K. Erlang in 1917 at the behest of the telephone company [*P. O. Elec. Eng. J.* **10**, 189 (1917)].

If $x = (\text{input rate})(\text{service time})$, then Erlang's formula for the reject rate P_c in c servers with no queue is

$$P_c = \frac{x^c / c!}{\sum_{k=0}^c x^k / k!}.$$

6.2. Far Detector

We assume for the time being a conservative value of 6 μs for the readout deadtime of a single PMT for the IDE option. Then the rejection rate for any pixel is the PMT rate times the deadtime. For a nominal 1 kHz rate, dominated by noise and radioactivity, this gives a rejection rate of 0.6%, an acceptable value.

6.3. Near Detector

6.3.1. Target/Calorimeter Section

For the near detector, real neutrino events (and the muons that come from them) dominate the rate during the spill. To calculate deadtime effects, we need a model of the events. From NuMI-L-363 (Thomas and Wojcicki), we estimate that the number of CC neutrino interactions in the target/calorimeter is 1.8/m³/spill and that the number NC neutrino interactions is 0.6/m³/spill, for the high-energy beam. In addition, we assume that there are 1.8 muons/m²/spill coming from interactions upstream of the detector.

A reliable calculation of deadtime effects requires a detailed Monte Carlo. However, short of that, we can estimate the size of effects with a simple model. Take the shower section of an event to be 5 strips wide and 0.5 m deep and take the muon to be 2 strips wide and infinitely deep, but straight.

First, we calculate the rejection rate in this model with the discrete electronics option. We need only consider the shower portion of events in the target region, because we only need a time stamp for muon tracking, and that is effectively deadtime-free in the discrete case. An event will be compromised if there is an overlapping event in the 5 μs period prior to the event, since one or more strips will have a busy ADC. A target event will be sensitive to events in the region 0.5 m upstream of the start of the event to events 0.5 m downstream from the start of the target event, or to 1 m worth of events in the longitudinal direction. Transversely, target events will be compromised by events whose “left edge” is 4 strips to the left to events whose left edge is 4 strips to the right, or a total of 9 strips in each coordinate, or 72 cm total. In the direction along the strips, the target event is sensitive to the full 3-m length. Thus the volume of compromising events is 1 x (0.72 x 3 – 0.36²) = 2.0 m³. Thus, from our earlier assumption on rates, there will be 4.8 compromising events per spill. To this we have to add compromising muons from upstream events, both from outside the detector and from, on average, half the veto region. By a similar calculation, this gives an effective area of (0.48 x 3 – 0.24²) m² x 2.25

muons/m² = 3.1 muon events, for a total of (3.1 + 4.8) = 7.9 compromising events/spill. With a 5 μs deadtime and a 1 ms spill, this gives a 3.8% rejection rate.

If we used only one VA chip per PMT, the deadtime in the IDE option would be larger than that of the discrete solution because (1) we have estimated the effective readout time to be 6 μs compared to 5 μs for the discrete option, and (2) a whole PMT would be dead whenever one pixel had a signal. The calculation of the latter effect is somewhat involved, but the average effective dead region is 20.6 strips, or 0.82 m for events, and 20.1 strips, or 0.80 m for muons. These effects lead to an x value of $[1 \times (1.64 \times 3 - 0.82^2) \times 2.4 + (1.60 \times 3 - 0.80^2) \text{ m}^2 \times 2.25] \times 6 \mu\text{s}/1\text{ms} = .117$ and a 10.5% rejection rate.

The above value is for a NC event. A CC event would have additional deadtime due to the measurement of the muon. For the muon, an ADC value is relatively unimportant, as the main information needed is just the binary information of whether a muon hit a strip or not. In the discrete option, all of the time stamps are available unless two events occur within 150 ns, so this issue is not important. For the IDE option, however, the time stamp is for the PMT, and which strips share the time stamp is only determined by reading out the ADC. Thus, we need to consider the number of additional events the muons will encounter in the remainder of the calorimeter section (the spectrometer section will be treated separately below). A similar calculation to the one above gives an average width of 17.1 strips and an average depth of 1.25. Thus, the additional deadtime x value is $1.25 \times (1.37 \times 3 - 0.68^2) \times 2.4 \times 6 \mu\text{s}/1\text{ms} = 0.066$, for a total rejection rate in target/spectrometer region of 15.5%

The above value is clearly too large, and for this reason we are proposing the dual VA/ADC readout for this region. With the dual readout, the calculation changes completely. A signal one pixel does not cause deadtime does not cause deadtime for any of its neighbors, since the second VA/ADC channel will be live after a 150 ns trigger resolving time. Furthermore, the pixel is not dead for its own readout time, since any additional signal will be picked up in the second channel. Thus we should be able to resolve and get a reasonable ADC measurement on the second pulse within a few peaking times of the shaper. If we conservatively estimate the resolving time to be 2 μs, then the x value is the same as in the discrete case times the ratio of resolving time to discrete readout time, or 0.4. This gives a rejection rate of 1.6%.

An additional deadtime will occur if two signals appear in one PMT during the readout time. To estimate the size of this effect, we consider the region of the detector with the highest density of PMT hits, the last plane of the calorimeter, which from our previous assumptions, has 55 muons and 2 NC events per spill. Since there are 4 PMTs in each coordinate per plane, there is an average of 14.3 events per spill per PMT for an x value of 0.086 and, from the Erlang formula, a rejection rate of 0.3%.

Adding these two sources of deadtime together, the IDE option has a total rejection rate in the target/calorimeter region of 1.9% compared to 3.8% for the discrete option. It should be noted that time stamps will always be available to indicate which events had an incomplete readout, thus allowing uncertainties due to the deadtime to be minimized.

6.3.2. Spectrometer Section

The conditions in the spectrometer section are worse by more than an order of magnitude since (1) the strips are twice as long, (2) the signals are multiplexed by a factor of 4, and (3) the number of muons continues to increase. Each plane is readout by 1.5 PMTs. For simplicity, we consider only the region read out by one PMT. By our assumptions, there are now 221 muons per spill in each PMT. This seems too large, since we have not put any muon attenuation into the model. Instead, we use the result of NuMI-L-363, which has 130 muons per spill at the end of the spectrometer, but, to be conservative, we assume that all are read out by a single PMT. This gives 0.78 muons per 6 μ s readout time. If we only used dual VA/ADC chips in this section, then there would be a rejection rate of 15%. With three VA/ADC chips per PMT, the rejection rate drops to 3.7%.

While this would work, it is not a completely satisfactory solution. There are a number of solutions that we offer for consideration, in order of increasing desirability:

- (1) Increase the number of VA/ADC chips per PMT to four. Although this would reduce the rejection rate to 0.7% and be inexpensive, we are already sensitive to the third power of our assumptions, and we would become sensitive to the fourth power.
- (2) Since we are only really interested in time stamps, just read them out directly and eliminate the VA chips from this region. This solution seems ugly and there is some utility in having ADCs in this region, for example, to measure muon bremsstrahlung events.
- (3) Eliminate the four-fold multiplexing. This would only add 144 PMTs to the experiment. The rejection rate calculation would change to 0.2% for the three VA/ADC chip configuration or 2.7% for the dual VA/ADC configuration.

Finally, we note the need for good Monte Carlo calculations to verify these back-of-the-envelope estimates.

7. Appendix – Sept 24, '99

This section describes changes in the front end electronics which have taken place over the last month or so. The largest change, of course, is that the IDE readout is no longer proposed for the near detector, which is now based on the QIE chip. Note that this document is a simple introduction to the far detector electronics for the purposes of the Oct. 1 design review. It is by no means a complete spec.

7.1. Front end board

7.1.1. Mounting

The basic structure of the front end board is unchanged from the original (see Fig.5) The following mounting scheme is under consideration.

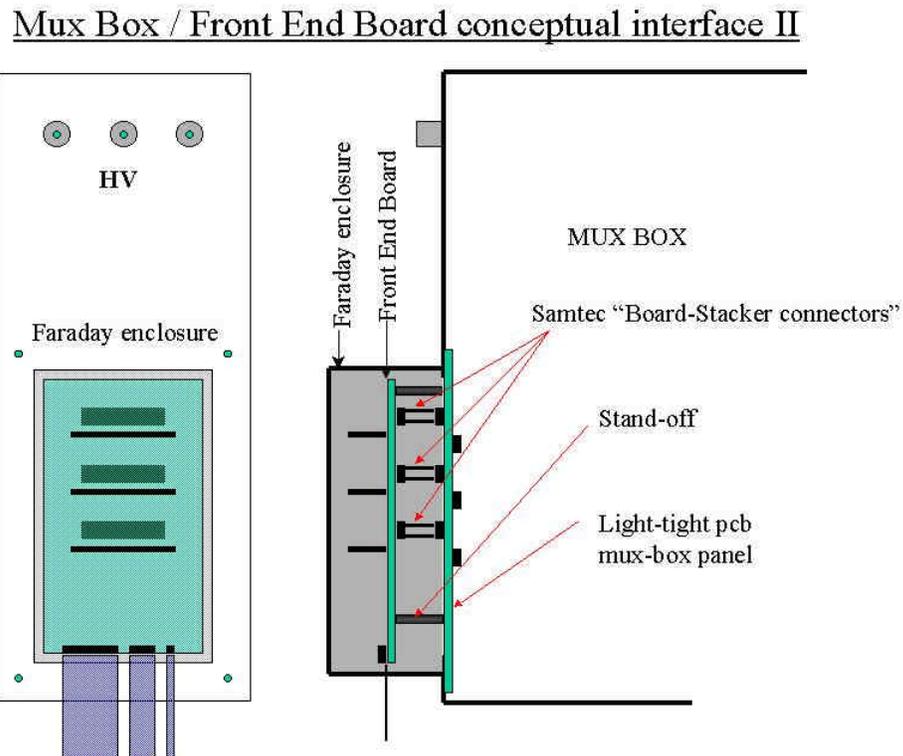


Figure 7 : mux-box / front end board

The idea is to have a printed circuit panel as an integral part of the mux-box. This panel contains connectors facing in to mate with ribbon connectors to the PMT base. It also has connectors facing out which mate with connectors on the

front end board using board to board connector hardware (eg Samtec “Board Stacker” series)

7.1.2. PIN diode inputs

We assume that there will be one pin diode to monitor for each PMT. Since its signal is expected to be much smaller than the PMT signal, it must be boosted in such a way as to produce a “PMT like” signal. This means that the amplifier output must be high impedance, low capacitance, and have a dynamic range compatible with the VA chip which will read it out on an unused channel. The calibration light path must also be arranged such that the amplified signal arrives at the VA chip in “reasonable” coincidence with the light in the associated PMT. This is required for proper triggering and we expect that an accuracy of +/- 25 ns will be adequate.

For grounding integrity, it is important that no single ended signals nor extraneous ground connection be made to the front end board or its enclosure. Therefore, the PIN diode as well as its amplifier will be mounted directly on the front end board. Light will be brought in by fiber optic. From our perspective, we view the PIN diode & amplifier as a single component and will provide connector space on the front end board for it. High speed is not a requirement for readout by the VA-chip and we favor designs which are low power and only enough speed for compatibility.

7.1.3. DC source monitoring.

A DC source monitor, by definition, monitors the product of a) the rate of source events, b) the average number of pe per source event, and c) the PMT gain. The Readout electronics in its normal mode of operation, provides a measurement of all three factors independently. The only limitation is the rate which we specify to be 10kHz max.

The VA chip is capable, in principle, of using its input calibration multiplexer to monitor dc current. However, this would require coordinating the input mux in some way, with the motor drive which handles the source scan.

The above two considerations led us, (us and Rich Talaga) to conclude that the dc source monitoring should be dropped from the spec.

7.1.4. Dynode trigger

The dynode signal, common to all sixteen channels, will be used to generate trigger signals. At $1e6$ PMT gain, the nominal single photoelectron pulse at the anode will be 160 fcou. On a low gain pixel, this could be down by 50% to ~80 fcou. If we assume the lowest dynode has gain of 2, then the minimum dynode signal will be at least 40 fcou. If dynode gain is 4, then this goes up to about 60 fcou.

The candidate device to process the dynode charge is “ASD-lite”, an amp/shaper/discriminator designed for ATLAS muon system. The device has the following characteristics.

- 0.5 micron CMOS, operating at 3.3 V
- 4 channels per chip, fully differential preamp/shaper/disc
- Digital output levels : LVDS
- $Z_{in} = 120$ ohms
- Shaper peaking time = 15 ns
- Sensitivity ≈ 12 mv /fc
- Enc ≤ 0.5 fc

Initial tests with this device show very good results. The device exists in undiced wafer form in large quantity and could be made available for MINOS if desired.

7.1.5. VA supplies and digital levels

The VA chip can be operated either at GND, +2V, and +4V, or using split rails at -2V, GND, +2V. There are some subtle differences due to the fact that the middle rail supplies the source current for the VA's input p-channel fet. This voltage rail, when viewed with respect to the stray capacitances seen by the VA input, has poor PSRR. In other words, lowest noise pickup is assured if the middle rail is coupled very tightly to the faraday enclosure of the mux-box and front end board since these constitute the “back plate” of all stray capacitance to the inputs. The best one can do in this case is to declare the middle rail to be “GND” and this forces us to use split rails. Of course the first option is also possible if one ties the middle rail (+2V) to the faraday cage capacitively using very good bypass capacitors and a very low inductance path.

The split rail choice does come with a penalty which is that it makes the digital interface more difficult and requires level shifting. For this purpose, an opto-isolated scheme is preferred by IDE. The additional cost for this is somewhere around \$2.50 per digital line, or in our case, about \$40 / front end board. None the less, we currently favor the split rail option as being more conservative.

7.2. Readout board

7.2.1. General features

The overall architecture of the readout board is shown below.

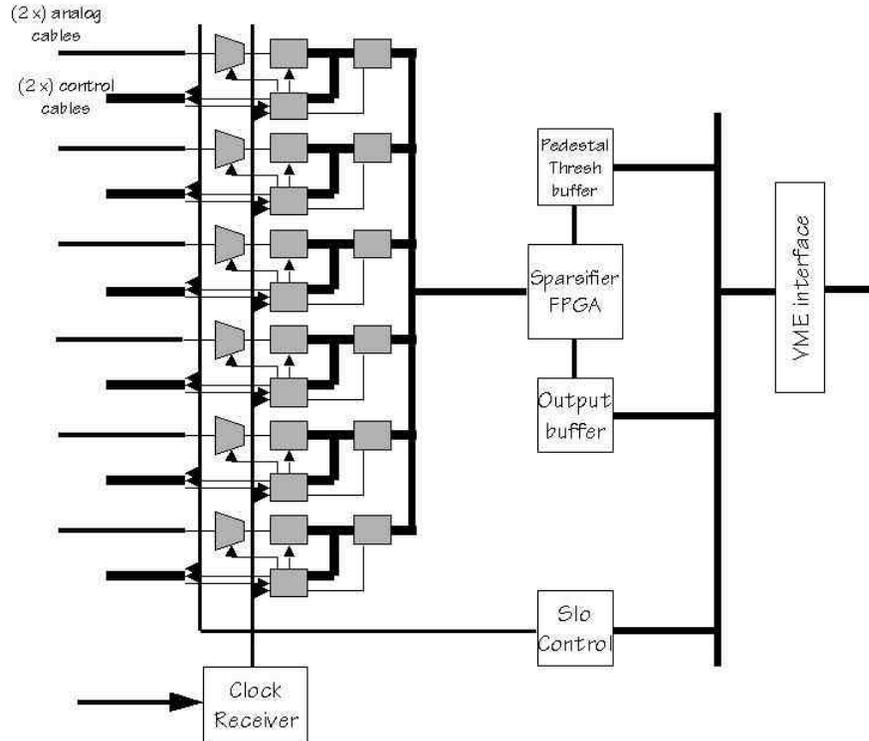


Figure 8 : Readout board architecture

Its “front end” is divided into six identical sections each of which has an ADC with 2:1 input multiplexer, a controller with time stamp, and an 18 bit-wide fifo. Each of these sections services two front end boards. This represents a change from our earlier description in which one ADC services one front end board. The reason for the change is the observation that in the original spec, each ADC is busy only 1.8% of the time. With no loss of readout rate, we can better utilize each ADC by having it service two front end boards keeping it busy 3.6% of the time. We could, in fact, further reduce the number of ADCs, but the cost savings diminish and in the interest of conservatism, we stop at six ADCs per board.

7.2.2. Cabling

The readout board will have twelve sets of cables going out to the twelve front end boards. Each set consists of

- Control cable : 50 conductor LVDS signals for independent control of 3 VA chips, 0.025” pitch, 30 ga.
- Analog cable : Double shielded (foil & braid), low dispersion expanded ptfе cable – Gore “QuietZone”
- Low voltage power cables : shielded twisted pairs as needed (See Grounding document for power connections)

7.2.3. Clock receiver

There are three global timing signals received by the board. All are transmitted to the board via LVDS signals on the backplane of the VME crate. They are generated by the Global Clock Receiver Module in the crate (Oxford). The received signals are

- 40 MHz CLK : Global timebase
- MARKER : One CLK period in duration, once per second
- CAL : Accurate (~ 1ns) signal to coordinate timing of cal-injection to front ends.

7.2.4. Time stamp & VA controller

The VA controller will handle following tasks

- Receipt of dynode triggers from front end boards; six triggers total
- Control of VA chip and coordination of ADC control lines
- Generation of internal 80 MHz clock and 27 bit course counter for time stamp. Course counter resets on receipt of MARKER signal once per second
- Generation of 4-phase internal clock for time stamp interpolator – 3.125 ns bins.
- Loading of 20 word data packet (shown below) into fifo

0	Header	1	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	SEL	VA1	VA0
1	Timestamp	0	0	Timestamp lower																	
2	Timestamp	0	0	Timestamp upper																	
3	ADC Data	0	1	x	x	ADC_ch0															
4	ADC Data	0	1	x	x	ADC_ch1															
5	ADC Data	0	1	x	x	ADC_ch2															
6	ADC Data	0	1	x	x	ADC_ch3															
7	ADC Data	0	1	x	x	ADC_ch4															
8	ADC Data	0	1	x	x	ADC_ch5															
9	ADC Data	0	1	x	x	ADC_ch6															
10	ADC Data	0	1	x	x	ADC_ch7															
11	ADC Data	0	1	x	x	ADC_ch8															
12	ADC Data	0	1	x	x	ADC_ch9															
13	ADC Data	0	1	x	x	ADC_ch10															
14	ADC Data	0	1	x	x	ADC_ch11															
15	ADC Data	0	1	x	x	ADC_ch12															
16	ADC Data	0	1	x	x	ADC_ch13															
17	ADC Data	0	1	x	x	ADC_ch14															
18	ADC Data	0	1	x	x	ADC_ch15															
19	ADC Data, End Of Record	1	1	x	x	ADC_ch16															

Figure 9 : Fifo data packet

Note that there are 17, not 16, channels of ADC data. The VA chip is wired in such a way that channel 0 is unbonded, while channels 1 – 16 are wired to the PMT anodes. The reason for the channel 0 connection is that this channel should never have data on it. In cases in which a single pe pulse follows very closely after a large multi-pe pulse, some cable dispersion may cause residual signal in the second pulse train. Observation of the channel zeros will allow this effect to be calibrated out. Note that this is in any case a small and rare effect and this feature may never be used. The sparsifier will normally suppress the channel zero data and it should rarely or never appear in the final data stream.

The VA controller will be implemented in a Xilinx Virtex series FPGA.

7.2.5. Sparsifier

The sparsifier will off-load the data fifos in round-robin fashion and pack the sparsified data into buffer memory for VME readout. This function will be implemented in a Xilinx FPGA, probably a Virtex series part. The output data will consist of 8 bytes per valid hit. Thus, compared with the 20 word (40 byte) data packets in the fifos, the compaction is 5:1. Data blocks will be reported to the DAQ via a status register blocks corresponding to time intervals as opposed to fixed size blocks. Thus, for example, blocks can be downloaded corresponding to 10 ms of data. The time interval will be programmable in 1 ms units.

7.2.6. VME interface

The VME interface will support VME64 block data transfers as well as more mundane operations all the way down to D16/A24. The latter will be useful for preliminary tests using LabView or other commercial operating environment. The interface will be implemented using the Cypress CY7C960/964 “Slave VME Interface Controller” chip set.

Minos Far Detector Grounding Proposal¹
J. Oliver
9-Sep-99

Electronics Racks will house the Readout Board Mini-Crate, the HV power crate, and low voltage power supplies for the Front End Board. There will be sixteen such racks, each of which services four Mux-Box Racks as shown in Fig. 1. There will be a **Global Ground** defined by a copper bar or large copper braid which connects the Electronics Racks together laterally as shown also in Fig. 1. The Global Ground may also be connected to Earth (embedded copper rod) at one point for safety purposes.

The Mux-Boxes in the Mux-Box racks are floating with respect to the rack frames or other local metal hardware. The Front End Boards are contained in metal boxes which are screwed to the Mux-Boxes. Thus, the Front End Board's **local ground** is one and the same with that of the associated Mux Box. The Front End Board may require several power supplies. Each supply voltage will come to it, along with its power return, via a shielded twisted pair with drain wire connected to the shield as shown in Fig. 2. Thus at the Front End Board, **local ground** (pc board ground plane), all power returns, and power cable shields are one and the same net.

Fig 3 shows low voltage power supplies at the Electronics Rack. Note that the return lines for these supplies **are not connected to the Global Ground** bar. The supply voltage cable shields (drain wires), however, **are connected to the Global Ground**. **Thus, the primary ground connection tying the Mux Box local ground to Global Ground is the power cable shield²**. Since all supply return current flows through the return lines, and none through the shields, there is no voltage drop across the shields. Thus, the potential at the Mux Box Crates should be zero wrt Global Ground. For safety purposes, we need to guarantee that in the event that the low voltage cables are not plugged in at the Mux Box racks, the low voltage supplies do not float up too much from ground. This can be done by a safety diode circuit between low voltage return and global ground. These will be such that they will not be active in normal operation and not cause ground loops.

Signals between front end board and readout board will all be differential. There is only one analog signal which will be differential and the digital ones will be LVDS. The analog signal will be transmitted via shielded twisted pair with shield directly tied to ground at the Readout board and ac coupled to local ground at the front end board. Thus there is no dc ground loop. The digital LVDS signals will be transmitted on flat ribbon cable which may or may not be shielded. If shielded, the shield is directly coupled only at the Readout board end and ac coupled at the front end board. A shield may well be unnecessary and expensive for this cable and may not be used. In this case, the common mode range of LVDS receivers along with the zero potential difference between the two cable ends should guarantee reliable operation.

¹ Much of this document is based on ATLAS global grounding policy and available through ATLAS notes

² We may want to consider a more substantial ground connection using a copper braid tied between Mux Box and Global Ground bar which follows cable tray to the Electronics Rack.

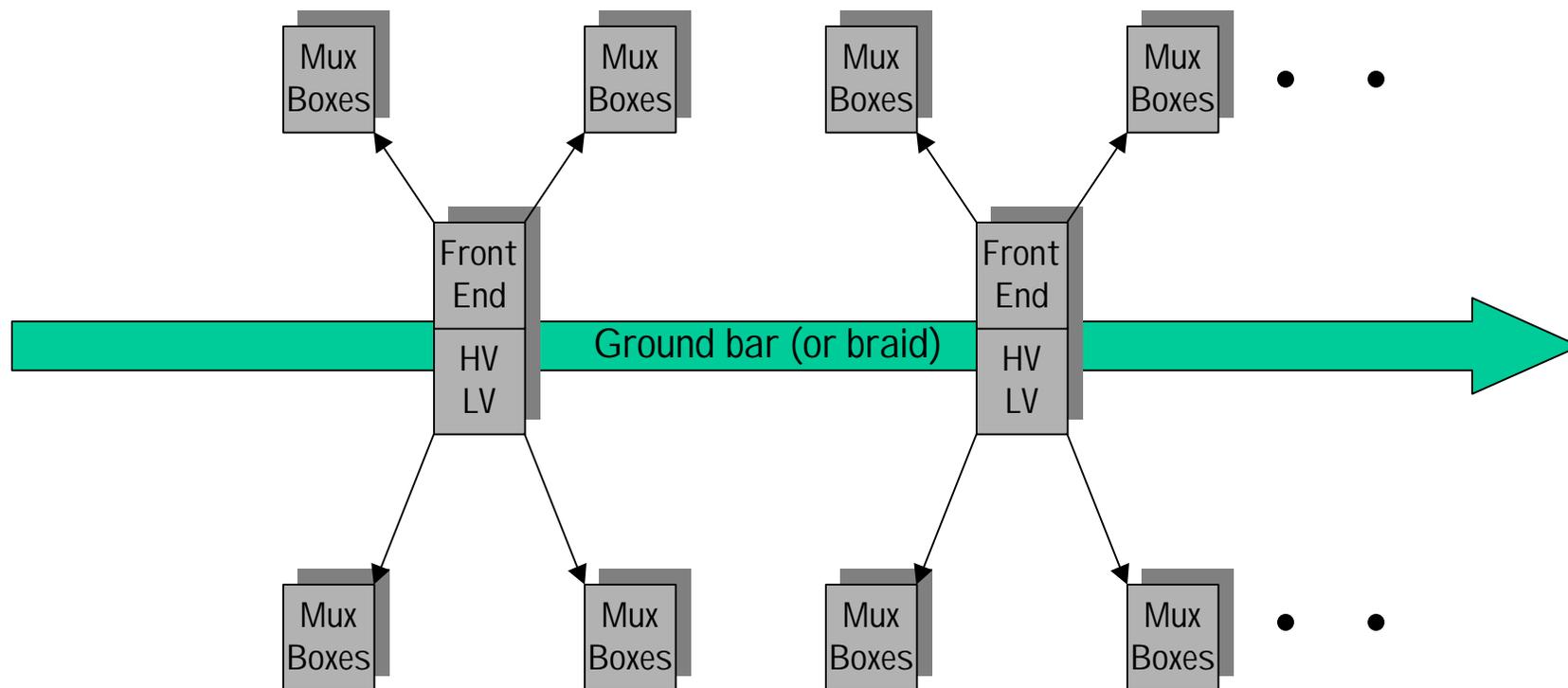
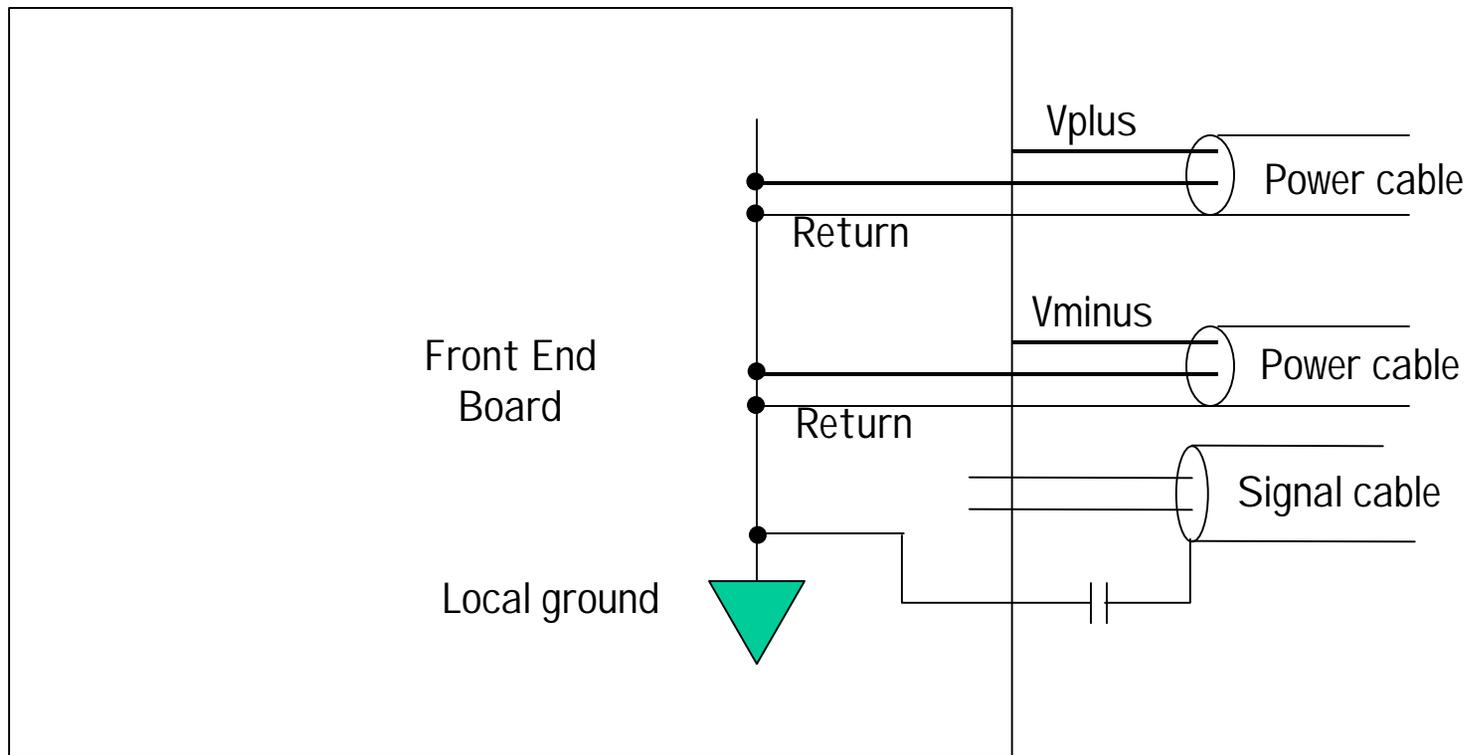


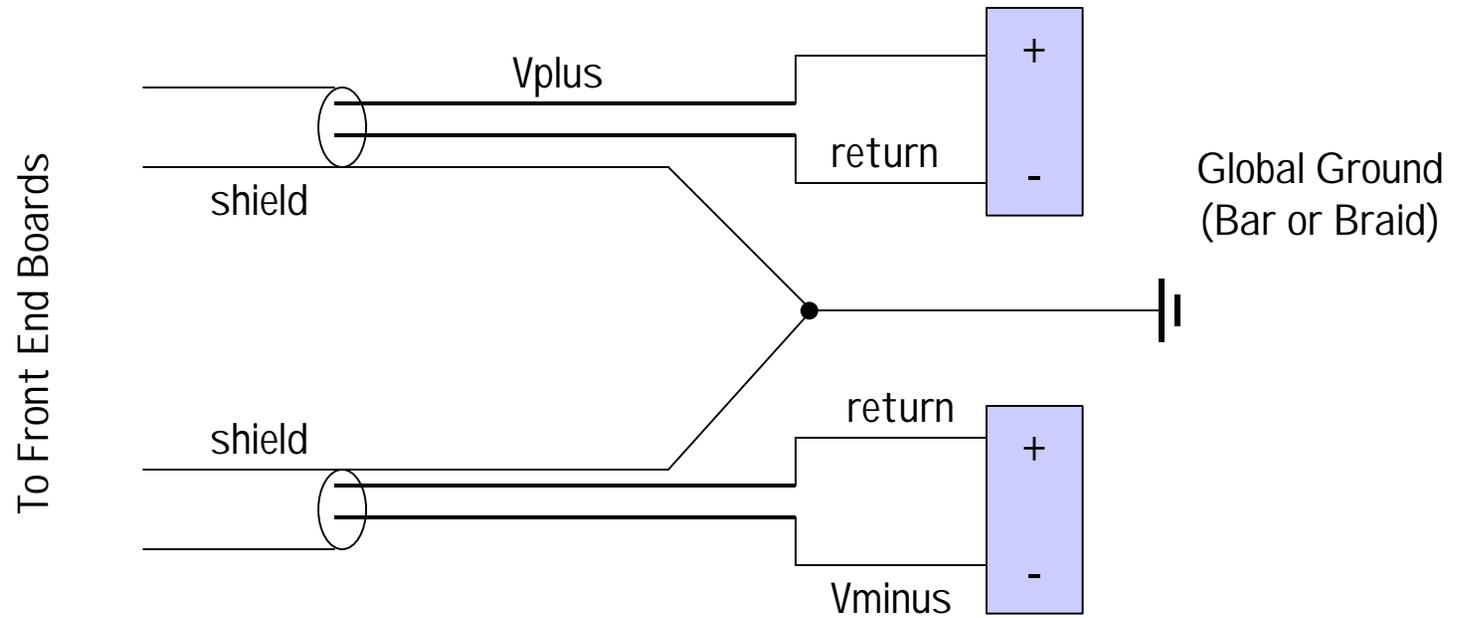
Fig 1

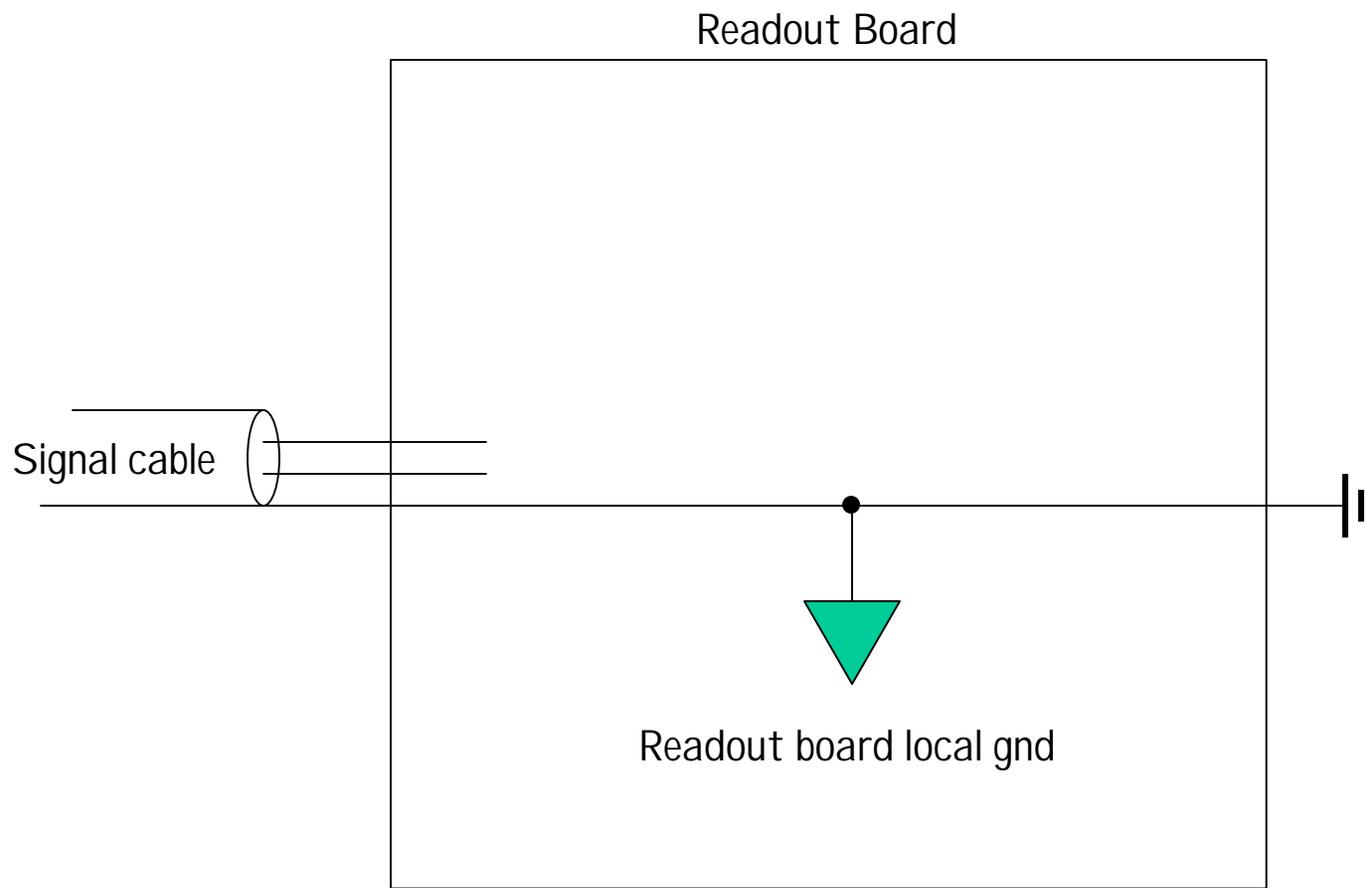


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Fig 2

Power supplies in Electronics Racks





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Fig 4

High voltage will be distributed from the hv supplies in the Electronics Rack along the same cable trays as the signal and lv supplies. The hv cables are assumed to be coax and thus single ended. In principle, one can break the ground connection at the Mux Box by using insulated SHVs and tying the SHV shell to local ground through a modest resistor of order several hundred ohms to 1 k ohm. This may or may not be necessary since even without this resistor, the ground loop created will be extremely tight, that is, very small in area since they use a common cable tray. I suspect the resistor connection will not be necessary but it may be prudent to reserve a place for it.

Finally, in order for this scheme to succeed, the following proviso needs to be enforced. **No additional ground connections for Detector Control, Calibration, or any other purposes may be made to the Mux Box local grounds.**